Nanotechnology, Science and Applications

Dovepress
open access to scientific and medical research

Open Access Full Text Article

ORIGINAL RESEARCH

A novel, efficient CNTFET Galois design as a basic ternary-valued logic field

This article was published in the following Dove Press journal:
Nanotechnology, Science and Applications
23 January 2012
Number of times this article has been viewed

Peiman Keshavarzian[1]
Mahla Mohammad Mirzaee[2]

[1]Kerman Branch, Computer Engineering Department, Islamic Azad University, Kerman, Iran; [2]Science and Research Branch, Computer Engineering Department, IA University, Kerman, Iran

Abstract: This paper presents arithmetic operations, including addition and multiplication, in the ternary Galois field through carbon nanotube field-effect transistors (CNTFETs). Ternary logics have received considerable attention among all the multiple-valued logics. Multiple-valued logics are an alternative to common-practice binary logic, which mostly has been expanded from ternary (three-valued) logic. CNTFETs are used to improve Galois field circuit performance. In this study, a novel design technique for ternary logic gates based on CNTFETs was used to design novel, efficient Galois field circuits that will be compared with the existing resistive-load CNTFET circuit designs. In this paper, by using carbon nanotube technology and avoiding the use of resistors, we will reduce power consumption and delay, and will also achieve a better product. Simulation results using HSPICE illustrate substantial improvement in speed and power consumption.

Keywords: galois field, CNTFET, MVL circuit design

Introduction

In the last few years there has been a considerable increase in nanotechnology research, especially nanoelectronics.[1] Carbon nanotube field-effect transistors (CNTFETs) have significant potential to replace metal-oxide semiconductor field-effect transistor (MOSFET) technology in the future, due to unique mechanical and electrical properties.

In order to sustain Moore's law and to ensure further improvements in FET performance, it is necessary to look for an alternative like CNTFETs, which promises to deliver much better performance than existing MOSFETs. CNTFET technology can also be easily matched with bulk complementary metal-oxide semiconductor technology on a single chip and utilize the same infrastructure.[1,2] Compared with binary logic, the multiple-valued logic (MVL) circuits provide better performance in chip size and speed. There are fewer interconnections and there is simpler realization of logical functions.[3]

In the last decades, considerable attention has been given to MVL circuit design because of all its benefits. MVL circuits have more than two logical levels, and depending on the number of levels, may have ternary (base = 3) or quaternary (base = 4) logic styles.[3,4]

In CNTFETs, the threshold voltage of the transistor is established by the diameter of the CNTs. Therefore, a multiple-threshold design can be achieved by employing CNTs with different diameters (which will be controlled by chirality) in the CNTFETs. A resistive-load Galois field with CNTFET-based ternary circuit design

Correspondence: Peiman Keshavarzian
Kerman Branch, Computer Engineering Department, IA University, Kerman, Iran
7635131167
Tel +98 913 198 4599
Fax +98 341 321 0051
Email keshavarzian@iauk.ac.ir

has been proposed.[5,6] Resistors are used to prepare voltage division. The design techniques that are discussed in this paper eliminate the need for large resistors by employing active load with p-type and n-type CNTFETs in ternary logic circuits.[7]

Arithmetic operations (addition and multiplication) in the Galois field are designed with a new technique through ternary logic gates based on CNTFETs. For arithmetic circuit designs, novel, efficient Galois field circuits based on CNTFETs are presented to speed up and reduce power consumption. Simulation Program With Integrated Circuit Emphasis (SPICE) results show substantial advantages in terms of speed and power consumption compared with previous implementations.

Carbon nanotube field-effect transistors

CNTFETs have been replaced with primitive silicon devices. An FET based on a single-walled carbon nanotube (SWCNT) was successfully fabricated and demonstrated to be able to operate at room temperature in 1991.[8] CNTFETs have attracted significant interest as the next-generation devices for nanoelectronics.

Figure 1A illustrates a one-dimensional SWCNT, which can be either metallic or semiconducting depending upon the arrangement of carbon atoms defined by their chirality, C_h (ie, the direction in which the graphite sheet is rolled) and magnitude with CNT diameter, as shown in Equations (1) and (2), respectively, where a is the graphite lattice constant (0.249 nm) and n_1 and n_2 are positive integers that specify the chirality of the tubes. SWCNT can be a sheet of graphite that is rolled up and joined together along a wrapping vector [Equation (1)], as shown in Figure 1B, where a_1 and a_2 are unit vectors.[9] The CNT is called *zigzag* if $n_1 = 0$, *armchair* if $n_1 = n_2$, and *chiral* otherwise.

$$C_h = \sqrt{n_1 \cdot a_1 + n_2 \cdot a_2} \quad (1)$$

$$D_{cnt} = C_h/\pi \quad (2)$$

Substituting the channel of a conventional MOSFET by a number of semiconducting CNTs is one of the particular details in CNTFET (shown in cross-section in Figure 2).[10] The major operation of CNTFET is the same as traditional MOSFET. Because the electrons are limited to the narrow nanotube, the mobility goes up substantially on account of ballistic transport, as compared with the bulk MOSFET.[11] Two types of CNTs are being extensively studied. One is a tunneling device (Figure 3A), which works on the principle of direct tunneling through a Schottky barrier at the source–channel junction.

The barrier width is modulated by application of the gate voltage, so transconductance of the device is dependent on the gate voltage.[12]

To overcome the disadvantages associated with the Schottky barrier, there have been attempts to develop CNTFETs that behave like normal MOSFETs. These attempts have had significant success so far and have enormous potential.

The MOSFET-like CNTFET (Figure 3B) operate on the principle of barrier height modulation by application of the gate potential. In this paper we will consider the non-Schottky barrier MOSFET-like unipolar CNTFET with ballistic transport as our device of interest. Hereafter in this paper the abbreviation CNTFET will be used to denote such

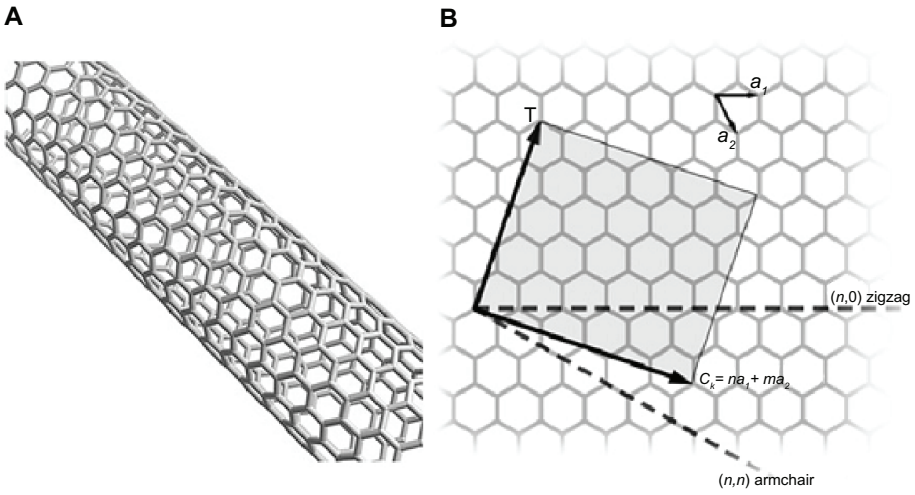

Figure 1 (**A**) Single-walled carbon nanotube and (**B**) graphite sheet in terms of chirality and n_1 and n_2.

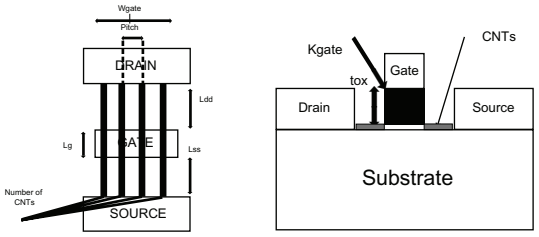

Figure 2 Schematic carbon nanotube field-effect transistors cross-section.

a MOSFET-like device unless otherwise stated (Figure 3B shows the band diagram of this device).[12–14]

The source Fermi level for a degenerately doped source can be derived from the conduction band edge. Inside the intrinsic channel, the Fermi level is in the middle of the bandgap. An important property of these CNTFETs is that the bandgap is inversely proportional to the diameter of the nanotube as shown in Equation (3).[15,16]

$$E_g = \frac{0.84}{d(nm)} ev \quad (3)$$

$$V_{th} = \frac{0.42}{d(nm)} ev \quad (4)$$

As the barrier height determines the threshold potential of an FET, the threshold voltage of the CNTFETs can be expressed as Equation (4).

This geometry-dependent threshold voltage has been exploited in this study to obtain CNTFETs that turn on at different voltages depending on their diameters. It is worth mentioning that the circuit realization of the ternary logic family involves dual transistors.

CNTFETs provide an opportunity to obtain two functional behaviors by using two different tube diameters. CNTFETs provide the unique opportunity of being controlled by changing the CNT diameter. Therefore, in this paper, we have used a dual-diameter CNTFET-based design for the ternary logic implementation to present ternary-valued logic Galois field circuit design.

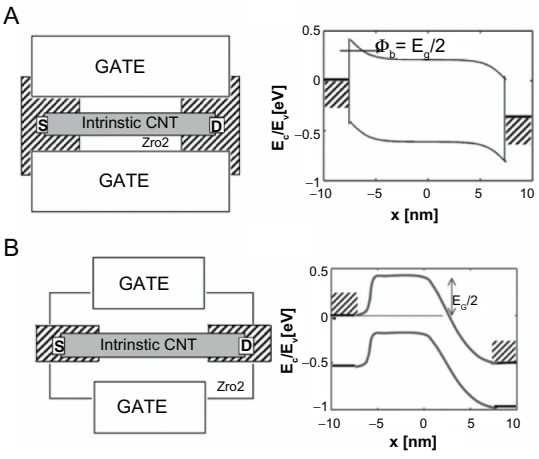

Figure 3 Two types of single-walled carbon nanotube field-effect transistors.

Review of ternary logic and Galois field

MVL circuits can reduce the number of operations necessary to implement a particular mathematical function and, further, have an advantage in terms of reduced area. In comparison with the fastest binary counterpart, chip area and power dissipation have been shown to be reduced using efficient MVL implementation.

Ternary logic gets special attention among MVLs. MVL is an alternative to common practice binary logic and has been expanded from ternary (three-valued) logic. By adding on a third value to the binary logic we have ternary logic functions that are significant. In this paper, 0, 1, and 2 denote ternary values to represent false, undefined, and true, respectively. Various fields with their unique characteristics and operators are described in MVL, such as literal, Galois, LukaSiewicz, Godel, and Kleene–Bochvar. Each field consists of a number of functions and basic operators such as addition and multiplication operators in the Galois field. Quaternary Galois field arithmetics contribute greatly to future computation in the field of MVL.[17,18] The quaternary inverter, successor, clockwise cycle, and counterclockwise cycle gates are proposed with the help of the all-optical quaternary Galois field adder circuit.[19]

Multi-output Galois field sum of product synthesis methods allow Galois-like circuits to be synthesized for realistic-sized multi-output functions.[20] Ternary Galois field sum of product expressions have been found to be a good choice for ternary reversible logic and particularly for quantum-cascaded realization of ternary functions.[21] The MVL functions should be implemented by a combination of the basic operators in the unique field area.[22–24] Although binary Galois field circuits have been investigated by many researchers, not much work has been done on MVL versions of such circuits. CNTFET is primarily concerned with circuits operating over three elements, such as the ternary Galois field (GF3).[5] A Galois field (F, +, ×) is a set with two operations that are closed with respect to that set. We will call them addition and multiplication.[5,25] A certain number of axioms ensure the existence of neutral (0 for the addition operation and 1 for multiplication) and inverse elements with respect to both operations, as well as commutativity and distributivity of multiplication for addition,

and define the structure of the field. The operations "+" and "×" together with the set F are said to form groups (F, +) and (F − {0}, ×), where the group is defined as a set with the operation that is closed with respect to that set. The axioms of a group guarantee that there is a unique neutral element, as well as the inverse element for each member of the group. All fields, such as Galois fields, contain a finite number of elements. In the case of a field with a prime number of elements, both operations are defined as usual modulo addition and multiplication. In other cases, the operations are more complex. They are defined with respect to irreducible polynomials over a simpler field. This means that if we have a field with p^n elements, then the operations are defined using some irreducible polynomial of degree "n" over the field with "p" elements. The ternary-valued logic Galois field multiplier and adder are introduced as they are inspected (Tables 1 and 2).

For each combination of inputs, unique and appropriate stable output should appear in the output node to define the Galois field multiplier and adder.

CNTFET-based Galois field circuit design

State-of-the-art design

Because many multiple-valued circuits over ternary Galois field can be synthesized using addition and multiplication operations in the Galois field as previously described, these basic operators can be used in multiple-valued implementations whenever they are applied. Put more simply, the MVL functions should be demonstrated by a combination of the basic operators in the Galois field. A CNTFET-based Galois field circuit design has been proposed.[5] It employs dual-diameter N-CNTFETs and resistors. Figure 4 shows the Galois field circuit design. It consists of several CNTFETs with resistive pull-ups. The simulation results described by Keshavarzian and Navi[5] are applied with 0.8 V as their supply voltage. Therefore, logic "0" corresponds to a voltage value less than 0.3 V, logic "1" depicts a voltage value between 0.3 V and 0.6 V, and the voltage values greater than 0.6 V are logic "2".

Table 1 Galois field adder

Addition	0	1	2
0	0	1	2
1	1	2	0
2	2	0	1

Table 2 Galois field multiplier

Multiplication	0	1	2
0	0	0	0
1	0	1	2
2	0	2	1

In Figure 4, there are two types of transistors with different diameters, d1 = 1.487 nm and d2 = 0.783 nm, with threshold voltages V_{th1} = 290 mV and V_{th2} = 550 mV, respectively.

When the input voltage is lower than 300 mV, all the transistors are off, and the output voltage is 800 mV. As the input voltage increases, $V_{th1} = 0.25V < V_{input} < V_{th2} = 0.58V$, just one of the transistors will be turned on and the other transistors will be turned off. The output voltage is held approximately at $V_{dd}/2$ until the input voltage reaches V_{th2}. Once the input voltage exceeds V_{th2}, both T1 and T2 are on and the output voltage is pulled down to nearly 0. However, as is shown in Figure 4, two resistors (greater than 100 KΩ) are required. The resistor values in the study by Keshavarzian and Navi[5] are too large to be integrated into CNTFET technology.

In terms of design,[5] the pull-up resistance was encountered in our design with the permanent output value (V_{dd}), which should be reduced to approximately zero when we should have zero at the output node. We have to control this permanent value by controlling all the other circuit elements. This problem would deteriorate our circuit design parameters such as delay, power, and power delay product (PDP).

The latest Galois field circuit design (Figure 5) for ternary logic implementation includes N-CNTFET and P-CNTFET with resistive pull-ups.[6] For each combination of inputs, only one predominant output path is activated. Therefore, through our circuit design structure, the output is held at the expected stable voltage by appropriate voltage division. Hence, analyzing the latest design shows that output voltages are the result of voltage divisions, which are produced by combining these resistors and active transistors. The V_{dd} voltage in the improved Galois field design is 0.8 V, and consequently our nanotube transistors have two different diameters with two different threshold voltages.

Proposed design

In this novel ternary CNTFET circuit design technique, a complementary CNTFET network can be used to accomplish impressive performance and low power consumption, avoiding the use of resistors and reducing area

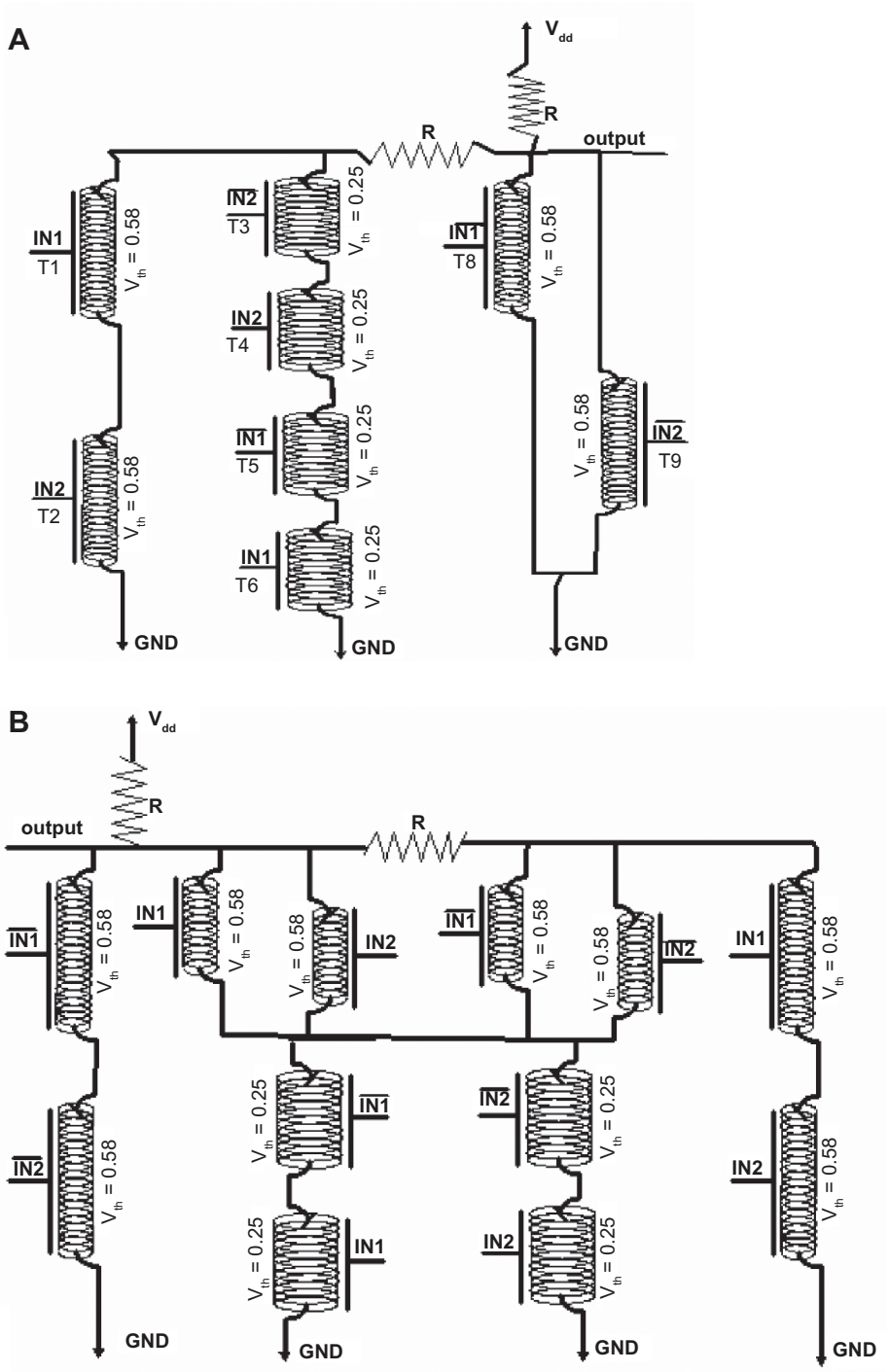

Figure 4 Efficient Galois field circuit design. (**A**) Galois field multiplier and (**B**) Galois field adder.

overhead. Figures 6 and 7 show the proposed CNTFET-based Galois field circuit designs to achieve two different threshold voltages with different chirality of the CNTs (19, 0 and 9, 0).

The diameters of transistors are 1.487 nm and 0.783 nm [Equation (2)]. Therefore, the threshold voltages of N-CNTFETs are 0.289 V and 0.559 V [Equation (4)].

The threshold voltages of P-CNTFETs are –0.289 V and –0.559 V. The novel, efficient Galois field circuits use a novel design technique for ternary logic gates based on CNTFETs that control all the paths by detecting each combination of inputs. Even the previous permanent pull-up voltage has been controlled by using P-CNTFETs without any resistors to achieve the best performance. Omitting resistive pull-ups and

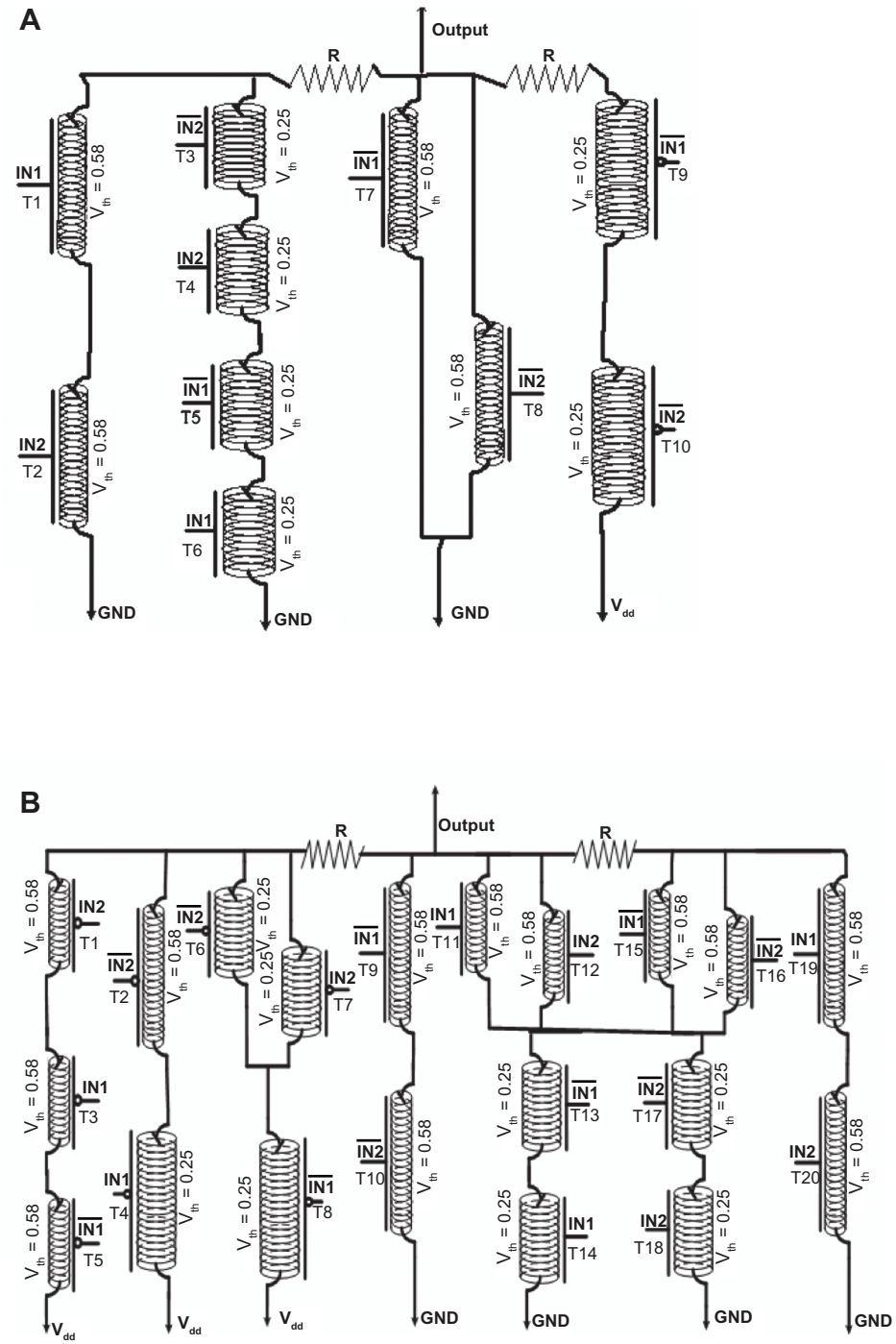

Figure 5 Improved Galois field circuit design. (**A**) Galois field multiplier circuit design and (**B**) Galois field adder circuit design.

controlling all the output paths restricts effects on the persistent V_{dd} value to the output and can achieve an improvement in circuit parameters such as delay, power consumption, and PDP. We added new P-CNTFET channels to prepare the voltage division instead of resistors in both designs (Galois field multiplier and adder) to appropriately activate our "V_{dd} to the output" path.

The V_{dd} voltage in the novel Galois field design is 0.8 V. If $V_{input} < V_{th} = 0.25$, all the N-CNTFET transistors will be turned off and P-CNTFETs will be turned on, and when the input voltage rises to $V_{th} = 0.25 < V_{input} < V_{th} = 0.58$, only the N-CNTFETs with $V_{th} = 0.25$ will be turned off. The P-CNTFETs with $V_{th} = 0.58$ V will be turned on and the others will be turned off. If input voltage rises further to

$V_{input} > V_{th} = 0.58$ V, all the N-CNTFET transistors will be turned on and all the P-CNTFETs will be turned off. Hence, analyzing our novel circuit designs shows that output voltages are the result of voltage divisions, which are produced by active transistors.[6] When in1 or in2 is less than 0.25 in the novel multiplier circuit design (Figure 6), T7 or T8 will be turned on and the output reaches 0 due to the only active connection to the ground. When in1 and in2 are more than 0.25, T9 or T10 will be turned on and these will activate the connection to the highest voltage (V_{dd}). If (in1, in2) = (1, 1)

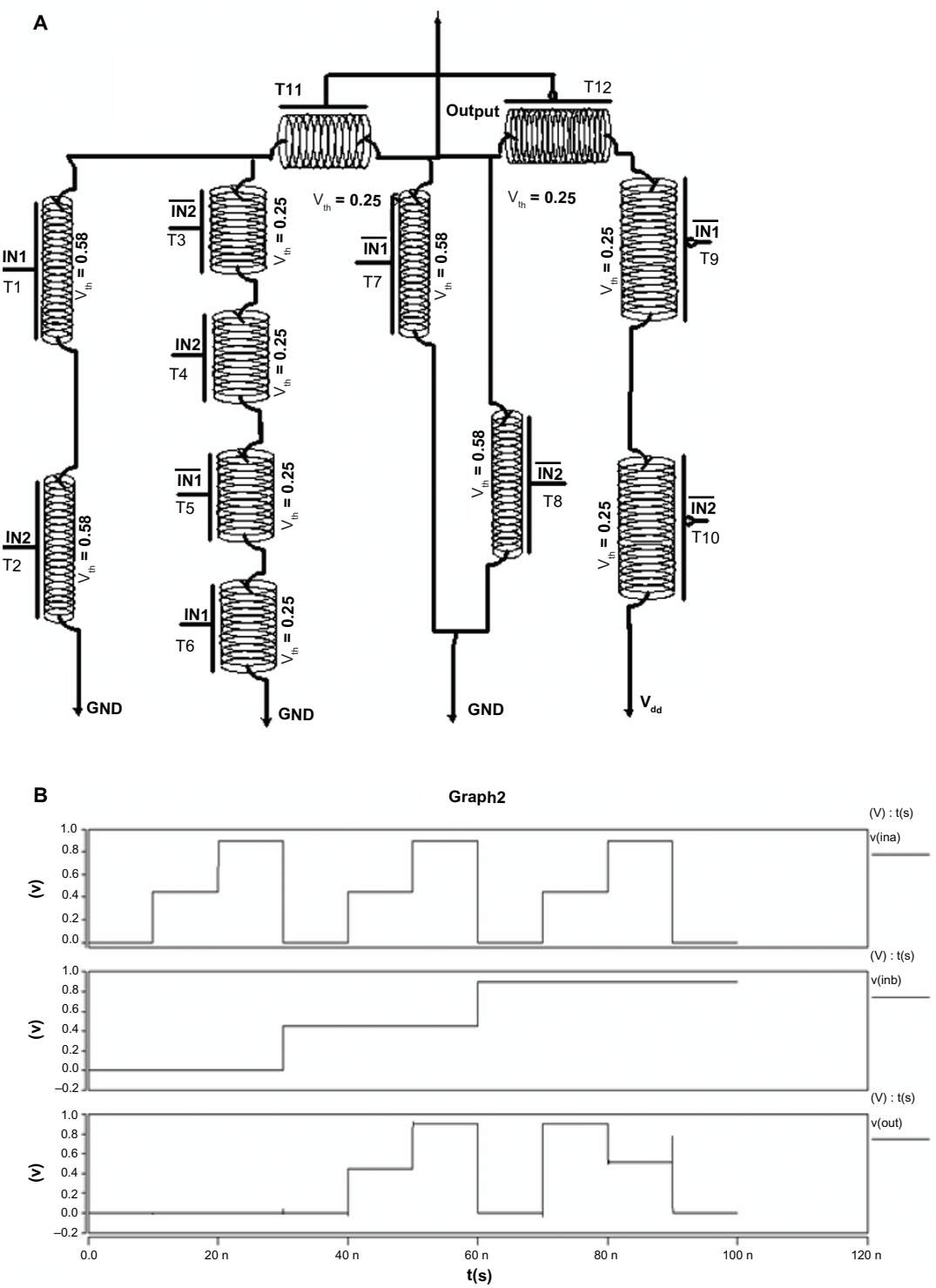

Figure 6 (**A**) Novel, efficient Galois field multiplier circuit and (**B**) simulation results of sample design.

or (in1, in2) = (2, 2), then we have the other active connections to the ground. Because of the resistors, we have a voltage division to achieve the expected voltage on the output node ($0.25 < V < 0.58$). If (in1, in2) = (2, 1), only the connection to the highest voltage is activated and others are disabled so that we have $V_{out} = V_{dd}$. In the novel Galois field adder circuit design (Figure 7), when (in1, in2) = (2, 1) or (in1, in2) = (0, 0), due to the active transistors, connection to the ground will be activated and the output reaches 0.

In the other combination of inputs, we will have the active connection to the highest voltage (V_{dd}) and also for (in1, in2) = ([1, 0], [0, 1], [2, 2]). In addition, we will have the other active connection to the ground so that these connections apply a voltage division resulting in ($0.25 < V < 0.58$) on the output node. For the other combination of inputs we have only one connection to the highest voltage (V_{dd}) and V_{out} will be equal to V_{dd}.

Simulation result with different supply voltages and temperatures

In this section, the proposed designs are simulated at different supply voltages and temperatures using

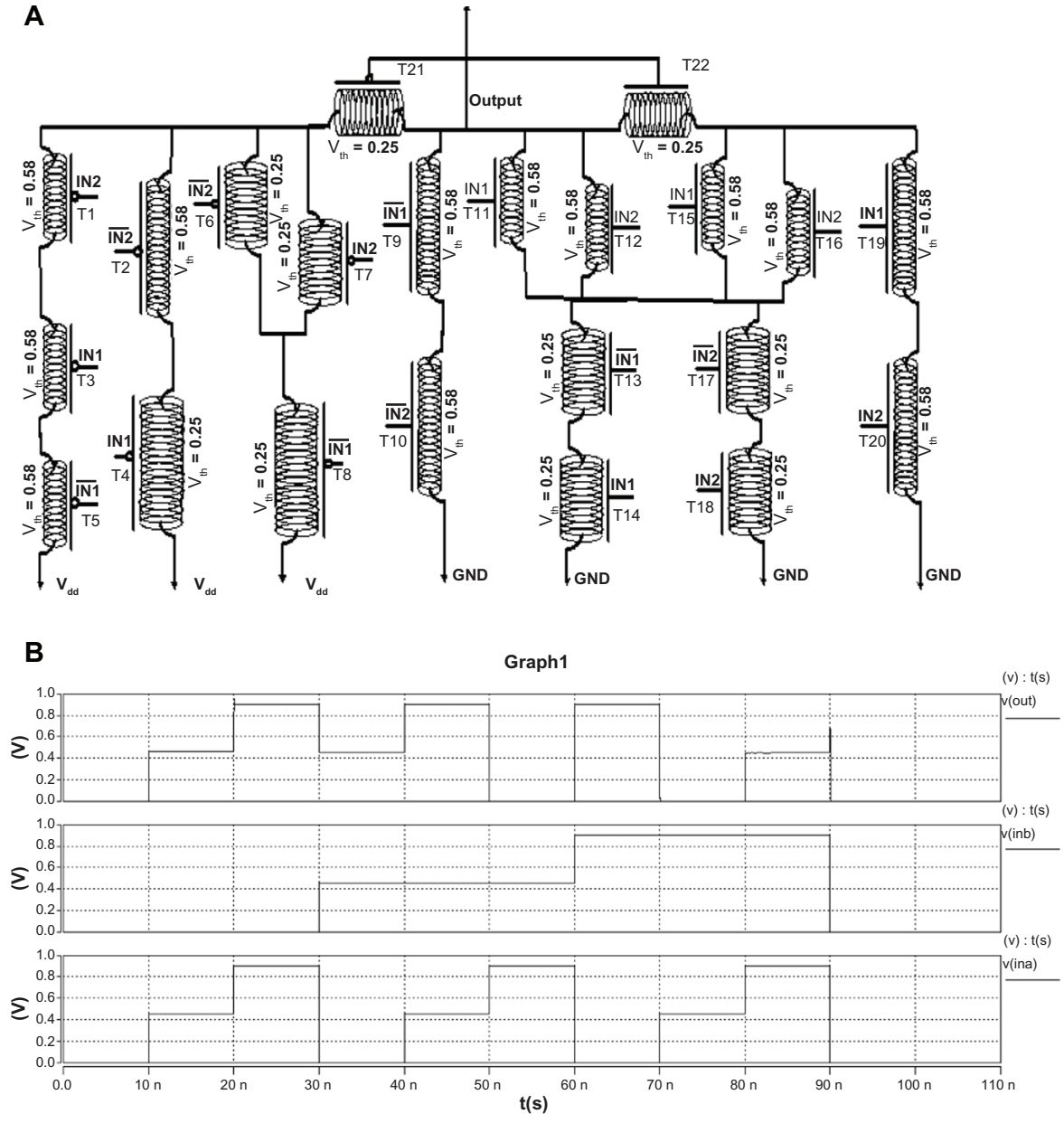

Figure 7 (**A**) Novel, efficient Galois field adder circuit design and (**B**) simulation results sample.

Synopsys HSPICE. In all situations, we measured average propagation delay and average power consumption. In order to make a trade-off between the delay and average power consumption parameters, the PDP metric was calculated, which is the multiplication of average delay and average power consumption. In the first experiment the circuits were simulated at 0.8, 0.9, 1, and 1.2 supply voltages and in the second one the circuits were simulated at the temperatures 0°C, 27°C, and 100°C. When the voltage of power supply increased, the simulation results show that the propagation delay decreased versus increasing power dissipation. By considering the effect of parameter variations with supply voltage (V_{dd}) as depicted in Figures 8–10, it was found that for the best performance, the supply voltage must be set at around 0.8 V. Reducing the supply voltage decreases the power consumption due to proportional scaling but also affects the circuit delay and PDP.

Changing V_{dd} results in a delay in V_{dd} = 1.2 V. In addition, the Galois field adder is 53.393%, 30.984%, and 17.8552% worse than the circuit design in V_{dd} = 1.2 V, for 0.8 V, 0.9 V, and 1 V, respectively. The Galois field multiplier is 53.4173%, 36.728%, and 24.94% worse than the circuit design in V_{dd} = 1.2 V for 0.8 V, 0.9 V, and 1 V, respectively.

As is shown in Figure 9, the best power is at V_{dd} = 0.8 V. In addition, the Galois field adder is 37.4942%, 64.652%, and 83.393%. The Galois field multiplier is 43.225%, 63.4994%, and 83.7% worse than the circuit design in V_{dd} = 0.8 V for 0.9 V, 1.0 V, and 1.2 V, respectively.

Figure 10 illustrates that we have the best PDP for adder and multiplier with V_{dd} = 0.8 V. In addition, the Galois field adder is 7.44%, 37.6995%, and 64.368% worse than the circuit design in V_{dd} = 0.8 V, for 0.9 V, 1.0 V, and 1.2 V, respectively. The Galois field multiplier is 22.9%, 43.9%,

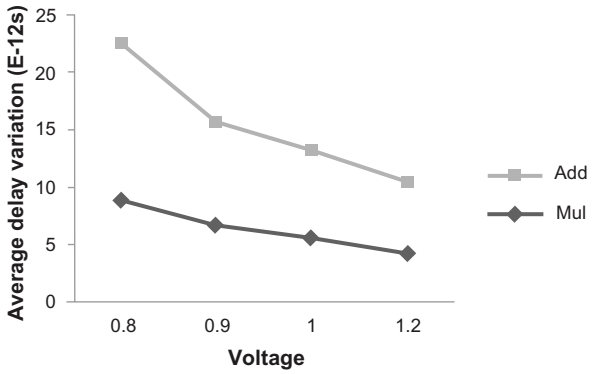

Figure 8 Variations of delay with supply voltage for Galois field circuit.

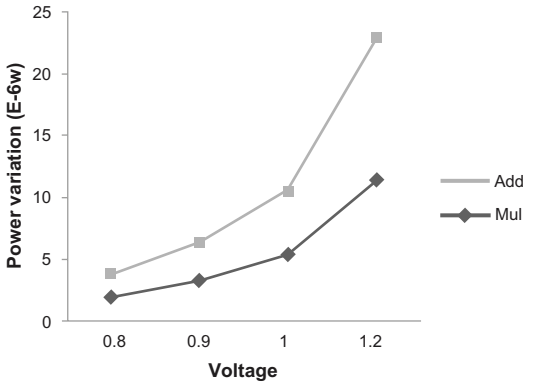

Figure 9 Variations of power with different supply voltage for Galois field circuit.

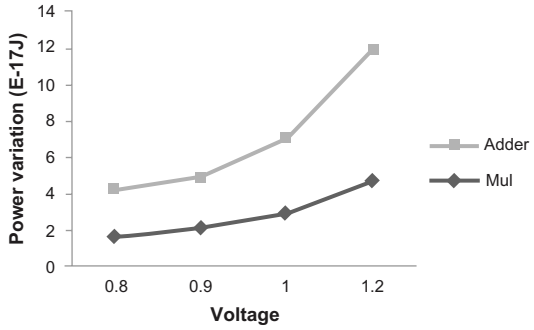

Figure 10 Variations of power delay product with supply voltage for Galois field circuit.

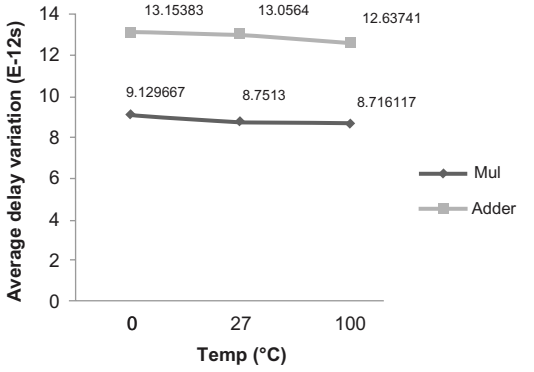

Figure 11 Variations of delay with different temperature for Galois field circuit.

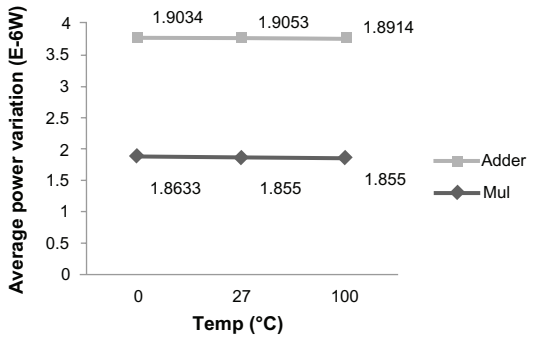

Figure 12 Variations of power with different temperature for Galois field circuit.

Table 3 Comparison results for Galois field adder

V_{dd} = 0.8 V	Average delay (pS)	Average power (μS)	Power delay product (J)
Galois adder[5]	52.9322	5.4082	2.8626×10^{-16}
Galois adder[6]	48.1699	4.0227	1.9377×10^{-16}
Proposed Galois adder	13.5564	1.9053	2.5829×10^{-17}

and 65.016% worse than the circuit design in V_{dd} = 0.8 V for 0.9 V, 1.0 V, and 1.2 V, respectively.

To test the immunity of the circuit to ambient temperature, noise and temperature variations, the designs are also simulated in three different temperatures, 0°C, 27°C, and 100°C.

The results achieved (shown in Figures 11 and 12) demonstrate that the proposed design has high performance and regular functionality in a massive range of temperatures. Figures 11 and 12 show that by increasing temperature, the delay and power consumption will be decreased.

Simulation results illustrate improvement in terms of power consumption, delay, and speed. We also use a novel technique to achieve an efficient Galois field circuit design. We compared our simulation results with the state-of-the-art Galois field CNTFET circuit designs.[5,6]

We present the performance evaluation of our new Galois field circuit design and compare it with previous designs. The comparison results are illustrated in Tables 3 and 4.

In the novel Galois field adder, we have achieved more than 71.857% improvement in terms of average delay and also more than 52.63% improvement in terms of average power, resulting in more than 86.67% improvement in the power delay product than the best Galois adder that has previously been proposed.[6]

In the novel Galois field multiplier, we have achieved more than 51.549% improvement in terms of average delay and also more than 44.20% improvement in terms of average power, resulting in more than 73.05% improvement in the power delay product than the best Galois multiplier that has previously been proposed.[6]

Table 4 Comparison results for Galois field multiplier

V_{dd} = 0.8 V	Average delay (pS)	Average power (μS)	Power delay product (J)
Galois multiplier[5]	46.5516	6.5086	3.0298×10^{-16}
Galois multiplier[6]	18.3156	3.3245	6.0890×10^{-17}
Proposed Galois multiplier	8.87395	1.855	1.6461×10^{-17}

Conclusion

In this paper we have presented an improved Galois field circuit design using CNTFETs. We achieved a significant improvement in delay, power, and PDP. This design controls all the three stable output voltage values by controlling the appropriate CNTFETs. To achieve an improved Galois field circuit design, all the CNTFETs have been used to activate the adequate guidance path and to disable all the other paths to the output without resistors. Thus, we have three stable voltage values on the output node.

Disclosure

The authors report no conflicts of interest in this work.

References

1. Yao Z, Postma HW, Balents L, Dekker C. Carbon nanotube intramolecular junctions. *Nature*. 1999;402:273–276.
2. Li WZ, Xie SS, Qian LX, et al. Large scale synthesis of aligned carbon nanotubes. *Science*. 1996;274(5293):1701–1703.
3. Mukaidono M. Regular ternary logic functions: ternary logic functions suitable for treating ambiguity. *IEEE Trans Computers*. 1986;C35(2):179–183.
4. Wu X, Prosser FP. CMOS ternary logic circuits. *IEEE Pro G El Circ Syst*. 1990;137:21–22.
5. Keshavarzian P, Navi K. Efficient carbon nanotube Galois field circuit design. *IEIC Electronic Express*. 2009;6(9):546–552.
6. Keshavarzian P, Navi K. An improved CNTFET Galois circuit design as a basic MVL field. *Smart Nanocomposite*. 2010;1:2.
7. Lin S, Kim Y-B, Lombardi B. Novel CNTFET-based ternary logic gate design. *Midwest Symp Circuits Syst*. 2009:435–438.
8. Iijima S. Helical microtubules of graphic carbon. *Nature*. 1991;345:56–58.
9. Tans SJ, Verschueren AR, Dekker C. Room-temperature transistor based on a single carbon nanotube. *Nature*. 1998;393:49–52.
10. McEuen PL, Fuhrer MS, Park H. Single-walled carbon nanotube electronics. *IEEE Tra On Nanotechnol*. 2002;1(1):78–85.
11. Avouris P, Appenzeller J, Martel R, Wind SJ. Carbon nanotube electronics. *Proceedings of IEEE*. 2004;91(11):1772–1784.
12. Hwang JS, Kim HT, Son MH, Oh JH, Hwang SW, Ahn D. Electronic transport properties of a single-wall carbon nanotube field effect transistor with deoxyribonucleic acid conjugation. *Physica E: Low-dimensional Systems and Nanostructures*. 2008;40(5):1115–1117.
13. Pourfath M, Ungersboeck E, Gehring A, et al. Numerical analysis of coaxial double gate Schottky barrier carbon nanotube field effect transistors. *J Comp Electron*. 2005;4:75–78.
14. Guo J, Javey A, Dai H, Datta S, Lundstrom M. Predicted performance advantages of carbon nanotube transistors with doped nanotubes source/drain. *Phys Rev B Condens Matter*. 2003;309:39.
15. Deng J, Wong HSP. A compact SPICE model for carbon-nanotube field-effect transistors including nonidealities and its application. Part I: model of the intrinsic channel region. *IEEE Trans Electron Devices*. 2007;54:3186–3194.
16. Deng J, Wong HSP. A compact SPICE model for carbon-nanotube field-effect transistors including nonidealities and its application. Part II: full device model and circuit performance benchmarking. *IEEE Trans Electron Devices*. 2007;54:3195–3205.
17. Chattopadhyay T, Roy JN. All-optical quaternary galois field sum of product (GFSOP) circuits. *Optik International Journal for Light and Electron Optics*. 2011;122(9):758–763.

18. Khan MHA, Siddika NK, Perkowski MA. Minimization of quaternary galois field sum of products expression for multi-output quaternary logic function using quaternary Galois field decision diagram. Proceedings of the 38th International Symposium on Multiple-valued Logic. *IEEE*. 2008:125–130.
19. Chattopadhyay T, Taraphdar C, Roy JN. Quaternary Galois field adder based all-optical multivalued logic circuits. *Applied Optics*. 2009; 48(22):E35–E44.
20. Khan MHA, Perkowski MA, Kerntopf P. Multi-output Galois field sum of products synthesis with new quantum cascades, Proceedings of the 38th International Symposium on Multiple-valued Logic. *IEEE*. 2003.
21. Keshavarzian P, Navi K. Optimum quarternary Galois field circuit design through carbon nano tube technology. 15th International Conference on Advanced Computing and Communications. *ADCOM*. 2007:214–219.
22. Khan MHA, Perkowski MA, Khan MR, Kerntopf P. Ternary GFSOP minimization using Kronecker decision diagrams and their synthesis with quantum cascades. *Journal of Multiple-valued Logic and Soft Computing*. 2005:567–602.
23. Keshavarzian P, Navi K. Efficient carbon nanotube Lukasiewicz circuit design. Proceedings of 3rd International Conference on Nanostructures. 2010:1022–1025.
24. Raychowdhury A, Roy K. Carbon-nanotube-based voltage-mode multiple-valued logic design. *IEEE Tran On Nanotechnology*. 2005;4(2):168.
25. Keshavarzian P, Navi K. Universal ternary logic circuit design through carbon nanotube technology. *Int J Nanotechnol*. 2009;6(10–11): 942–953.