



ORIGINAL RESEARCH

Hysteresis modeling in ballistic carbon nanotube field-effect transistors

Yian Liu1 Mateus S Moura² Ademir | Costa^{2,3} Luiz Alberto L de Almeida4 Makarand Paranjape¹ Marcio Fontana²

Department of Physics, Georgetown University, Washington, DC, USA; ²Department of Electrical Engineering, Federal University of Bahia, Salvador, Brazil; ³Federal Institute of Bahia, Santo Amaro, Brazil; 4Engineering, Modeling and Applied Social Sciences Center, Federal University of ABC, Santo André, Brazil

Abstract: Theoretical models are adapted to describe the hysteresis effects seen in the electrical characteristics of carbon nanotube field-effect transistors. The ballistic transport model describes the contributions of conduction energy sub-bands over carbon nanotube field-effect transistor drain current as a function of drain-source and gate-source voltages as well as other physical parameters of the device. The limiting-loop proximity model, originally developed to understand magnetic hysteresis, is also utilized in this work. The curves obtained from our developed model corroborate well with the experimentally derived hysteretic behavior of the transistors. Modeling the hysteresis behavior will enable designers to reliably use these effects in both analog and memory applications.

Keywords: ballistic transport, nanoscale device, solid-state device

Introduction

Recent advances in nanotechnology have enabled the development and use of carbon nanotubes as field-effect transistors (CNTFETs). These devices have advantages over traditional metal oxide semiconductor transistors, including higher circuit integration,¹ increased gain, and higher mobility. The device consists of a single-wall (SWCNT) or multi-wall (MWCNT) carbon nanotube acting as the channel of a field-effect transistor, connected to two metal source and drain electrodes, and has its drain current controlled by a gate electrode. In general, a positive gate voltage shifts the Fermi level of the carbon nanotube toward the conduction band while a negative gate voltage shifts the Fermi level toward the valence band.3

Hysteresis is a peculiar effect in CNTFETs and is observed when the gate voltage is swept in the forward and reverse directions, leading to a hysteretic effect that is difficult to predictably analyze due to the different nonlinear effects that are present. Hysteresis is typically related to charge injection from the carbon nanotube into the gate oxide dielectric, particularly at large gate bias, where the charges then become confined until the gate polarity reverses as a part of the voltage sweep.4 Mathematical models have been developed to characterize hysteresis behavior, such as the limiting-loop proximity (L²P),⁵ Preisach,⁶ and Jiles-Atherton⁷ models. However, using only these models individually has not generated accurate approximations for CNTFET drain current versus gate voltage or I_{sp} – V_G electrical characteristics primarily because they do not take into account the specific properties of the nanotube. One theoretical model often used to describe CNTFETs was proposed, 8 based on the physical effects of ballistic conduction, wherein electrons in the nanotube are not affected by scattering. Ballistic transport has nearly been achieved in CNTFET

Correspondence: Marcio Fontana Department of Electrical Engineering, Federal University of Bahia, Salvador, 40210-630, Brazil Email mfontana@ufba.br

how to request permission may be found at: http://www.dovepress.com/permissions.php

Liu et al Dovepress

modeling by the use of proper contact materials such as palladium and gold, thereby reducing transport barriers and approaching the theoretical conductance limit of the device $(G_{ON} \approx 4q^2/h)$.¹⁰

The main objective of this work is to develop a reliable mathematical model by which to determine drain current by considering the physical basis of CNTFET conduction, which includes the hysteresis effect. Positive results were obtained, considering that some fitting parameters required estimation while instrument accuracy affected some of the obtained values. The results demonstrate that hysteretic effects can indeed be modeled and can potentially be used in a controlled manner for a variety of applications.

In this paper we describe the ballistic theory pertaining to carbon nanotube transistor behavior, including the relationship between V_G , V_{SD} , I_{SD} , and the transfer characteristics of the CNTFET. Adaptations to the L²P model to account for hysteresis, based on ballistic theory, are presented. We will also show the experimental procedures, methods, and materials used in order to obtain the device and data; explain the methodology used for the acquisition of the model parameters; present the results for different experiments and compare the data with simulations from the adapted model; and express conclusions about these comparisons.

Model description

Due to its dimensions, a carbon nanotube can be considered a quasi one-dimensional element, whose diameter and chirality directly affect its properties. There is no boundary scattering in pristine nanotubes due to the lack of surface bonds and a cylindrical structure. Thus, for long-length nanotubes, quasiballistic transport can be observed. 11,12

For a CNTFET, when contact is made between the carbon nanotube and the metal electrodes, a potential, or Schottky barrier is formed at the metal—carbon nanotube junction. This barrier has a height related to the work function of the metal electrode. Since gold was used as the contact material in this study, having a large work function, the Schottky barrier height became small. Hence, in this paper, we only consider the ballistic transport within the carbon nanotube channel and assume that the gate voltage only modulates the energy bands of the carbon nanotube channel between the source and drain.⁸

The channel potential can be described as:

$$\varphi_s = V_G, \text{ for } V_G < \Delta 1$$

$$\varphi_s = V_G - \alpha(V_G - \Delta 1), \text{ for } V_G \ge \Delta 1$$
(1)

where φ_s is the channel potential, V_G is the gate bias, α is the slope of the drain current curve, and $\Delta 1$ is the equilibrium sub-band minima of the first sub-band.

In order to remove the discontinuity at $\Delta 1$, the following equation is proposed:¹³

$$\varphi_s = V_G - \frac{\alpha(V_G - \Delta 1) + \sqrt{(\alpha(V_G - \Delta 1))^2 + \varepsilon^2}}{2}$$
 (2)

with ε serving as a smoothing parameter (typically around 0.5 V).

The slope of the characteristic curve, α , is expressed as a polynomial of V_{SD} such that $\alpha = \alpha_0 + \alpha_1 V_{SD} + \alpha_2 V_{SD}^2$, where α_0 , α_1 , and α_2 are dependent on both CNTFET diameter, d, and gate oxide thickness, t_{ox} . ¹⁴ The drain current, I_{SD} , can now be determined by the simplified expression below:

$$I_{SD} = \frac{4qkT}{h} \left[\ln\left(1 + e^{\xi_S}\right) - \ln\left(1 + e^{\xi_D}\right) \right]$$
 (3)

where

$$\xi_s = \frac{\varphi_S - V_{TH}}{V_t} \tag{4}$$

and

$$\xi_D = \frac{\varphi_S - V_{TH} - V_{CN}}{V_t} \tag{5}$$

thermal voltage

$$V_t = \frac{kT}{q} \tag{6}$$

where V_{TH} is the threshold voltage, k is the Boltzmann constant, q the electron charge, and T the temperature.

Hysteretic effects cause a shift of the threshold voltage, which may be considered as the first sub-band, Δ_1 . Experimentally, a sweep to large positive values of V_G creates a positive shift in the threshold voltage, ¹⁵⁻¹⁷ and V_{SD} does not affect the shift or the position of the curves. According to the variables set forth in the L²P model, ⁵ hysteresis is characterized by a horizontal shift between the two curves, denoted as w, which designates the magnitude of shift around a central voltage, V_C , along the horizontal axis. An auxiliary variable, δ , can be used to identify hysteresis orientation. These variables are experimentally obtained. In the case of CNTFETs, without these parameters shown

above, the current model cannot show hysteresis. Adapting the threshold voltage to L²P model variables, these effects are evidenced.

Applying these definitions:

$$V_{TH}(w, V_C) = \delta \frac{w}{2} - V_c \tag{7}$$

with

$$\delta = \begin{cases} +1, \text{ for } \frac{dV_G}{dt} > 0 \\ -1, \text{ for } \frac{dV_G}{dt} < 0 \end{cases}$$
 (8)

Although carbon nanotubes are described as having ballistic behavior, the contact resistance between the electrode and the carbon nanotube 18 affects the on-state current level because the drain-source voltage in the nanotube is just a fraction of V_{SD} applied to the transistor:

$$V_{CN} = \frac{R_{CN}V_{SD}}{R_{CN} + R_D + R_S} \tag{9}$$

where R_{CN} is the intrinsic resistance for the carbon nanotube, which is determined as $h/4q^2$ (approximately 6.4 k Ω), while R_D and R_S are the drain and source contact resistances, respectively.

Figure 1 illustrates the conceptual procedure for CNT-FET modeling, where w and V_C are obtained from the L²P model while the other variables arise from the ballistic model.

Experimental procedure

Silicon wafers (p-type, orientation <100>, 500–550 μm thickness, 0.001-0.005 Ω·cm resistivity) produced by NOVA Electronic Materials Ltd (Flower Mound, TX, USA) were used in this work. Thin silicon dioxide (SiO₂) layers were grown on the wafer by a typical dry-wet-dry oxidation process at a temperature of 1,100°C for 10 minutes, 70 minutes, and 10 minutes, respectively. Prior to the catalyst spinning procedure, the silicon wafer was cut into samples measuring 10×10 mm, which were ultrasonically degreased in trichloroethylene (C,HCl₃), acetone ((CH₃),CO), and isopropyl alcohol (C₂H_oO), rinsed in deionized water, and dried in nitrogen. A solution of ferric nitrate nonahydrate (1.6 mg) + precursor MoO₂(acetylacetonate ligand)₂ complex (0.5 mg) + aluminum oxide (15 mg) dissolved in methanol (20 mL) was used as the catalyst for carbon nanotube growth. Catalyst islands are patterned, using electron beam lithography and lift-off on boron-doped silicon substrates with 300 nm SiO, grown by thermal dry oxidation. SWCNTs are grown from these catalyst islands using chemical vapor deposition with a methane and hydrogen gas mixture (total flow 60 sccm) in a 750°C-900°C-750°C three-zone furnace set. The SWCNT samples were grown with methane flow (32 sccm) and hydrogen flow (28 sccm). After imaging as-grown nanotubes with a field-emission scanning electron microscope, source/drain electrodes are patterned by electron beam lithography. The width of the source and drain metal electrodes are 1 µm with a 1.5 µm separation. The metals chromium and gold (thicknesses of 30 Å/1,000 Å) are deposited by sputtering and followed by lift-off in acetone.

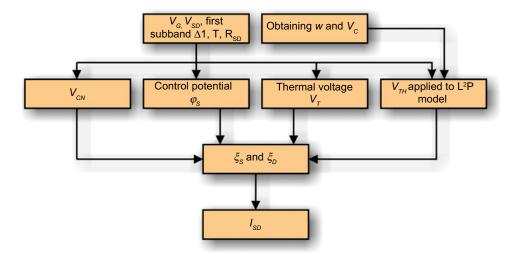


Figure I Flowchart for carbon nanotube field-effect transistor modeling.

Surface morphology of the grown layers was examined by field-emission scanning electron microscopy using a Zeiss SUPRA 55-VP FESEM microscope (Carl Zeiss Meditec AG, Jena, Germany). Micro-Raman spectroscopy was carried out at room temperature using a Renishaw Raman microscope (inVia; Renishaw, Wotton-under-Edge, UK) employing the output of an Ar+ laser (20 mW power) for excitation at λ =514.5 nm. A LabVIEW 2013 SP1 software program (National Instruments Corporation, Austin, TX, USA) was implemented in an IEEE-488 environment, using a computer to control the Model 4140B pA meter/DC voltage source (Hewlett-Packard Inc., Palo Alto, CA, USA), and connected to a four-probe micromanipulator system for characterization of device parameters. All devices were measured at room temperature (300 K) in a controlled pressure (1 atm + 0.12 kPa in H₂O) and humidity (30%) environment.

Model parameters identification

For the determination of the L²P model parameters w and V_C , we used graphic analysis based on the simulation results. Figure 2 describes the link between these parameters and their visual representation in the theoretical model. w is the horizontal distance between the two curves, obtained by tracing two lines in parallel with the inclination of the curves in their transition regions. Thereafter, V_C is obtained by determining the horizontal midpoint of w at the vertical point located in the off-state saturation current value.

Although α_0 , α_1 , and α_2 are inherent to the physical characteristics of the CNTFET, as mentioned in the Model Description section, there is no known mathematical relation that could allow the prior acquisition of these parameters. Thus, we considered each transistor as a stand-alone device,

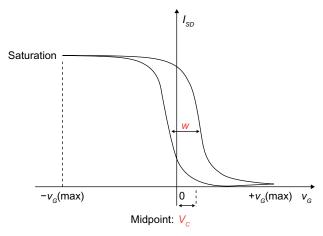
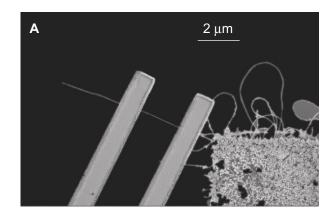


Figure 2 $I_{\rm SD}$ – $V_{\rm G}$ curves with hysteresis and obtainment of parameters w and $V_{\rm C}$. **Notes:** $I_{\rm SD}$ is the drain current; $V_{\rm G}$ is the gate voltage; w represents the horizontal shift between the two curves; and $V_{\rm C}$ represents the horizontal midpoint of w at the off-state saturation.

obtaining the slope of the curve in the transition region for each device and drain-source voltage by the minimization of deviations between the data and the model curves in this region. In this way, with at least three measurements of α for different values of V_{SD} , it is possible to determine α_0 , α_1 , and α_2 , for a device by a linear system.

Results and discussion

Figure 3A shows a long and straight single semiconducting nanotube contacted by two gold electrodes to form a CNT-FET, and Figure 3B illustrates the typical hysteresis behavior of the nanotube transistor for drain current versus gate voltage (with V_{so} =0.02 V). Data were taken at room temperature and



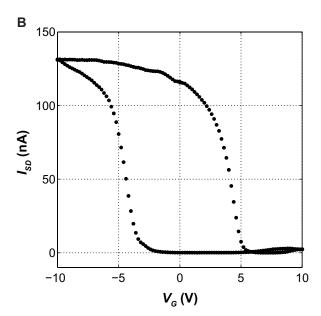


Figure 3 Fabrication and characterization of CNTFET.

Notes: (**A**) Typical field-emission scanning electron microscope morphology of the carbon nanotube field-effect transistor with 300 nm silicon dioxide grown by thermal dry oxidation and source and drain metal electrodes (chromium and gold with thicknesses of 30 Å/I,000 Å). (**B**) Typical hysteresis behavior of the carbon nanotube field-effect transistor at room temperature. Variables used are the drain current (I_{sp}) and the gate voltage (V_c) .

Abbreviation: CNTFET, carbon nanotubes as field-effect transistors.

the device is operated with gate voltages between $-10 \text{ V} < V_G < +10 \text{ V}$, in the asymmetric hysteretic transition region. This result corroborates well with the data from a previous work, ¹⁹ in which the CNTFET also showed that the device conductance was increased for negative gate voltages. We used the ballistic transport model⁸ and L²P model⁵ for hysteresis modeling of CNTFETs. Due to the effect complexity, this modeling is susceptible to nonlinearities, so we have incorporated effects in our model to include energy bands, memory phenomena, minor loop accommodation, and stabilization.

Figure 4A and B, respectively, show typical Raman spectrum and typical radial breathing mode peaks ranging from 100 to 300 cm⁻¹ that were used to estimate the diameter of the SWCNT.²⁰ We observed two typical SWCNT peaks located at 1,350 cm⁻¹ (D-band) and 1,590 cm⁻¹ (G-band). Table 1 shows details of the diameter distribution of SWCNTs synthesized in the furnace. The diameter distribution of the carbon nanotubes ranged between 1.0 nm and 2.2 nm depending on the different

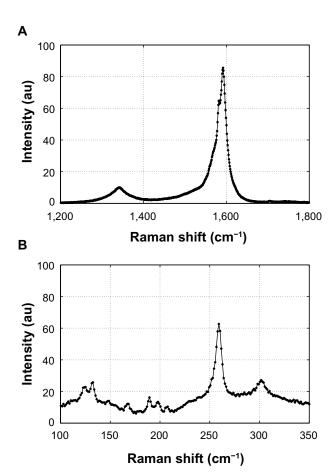


Figure 4 Raman spectra of the SWCNT.

Notes: (A) Typical Raman spectrum of the single-wall carbon nanotube. (B) Typical radials the athing mode peaks which were used to estimate the diameter of the single-wall carbon nanotube.

Abbreviation: SWCNT, single-wall carbon nanotube.

Table I The diameter distribution of single-wall carbon nanotubes synthesized in the furnace

| RBM bands | Diameters | Relative intensity | | |
|---------------------|-----------|--------------------|--|--|
| (cm ⁻¹) | (nm) | of the RBM | | |
| 124 | 2.2 | Weak | | |
| 133 | 2.1 | Medium | | |
| 148 | 1.8 | Weak | | |
| 167 | 1.6 | Medium | | |
| 189 | 1.4 | Medium | | |
| 198 | 1.3 | Weak | | |
| 208 | 1.2 | Weak | | |
| 259 | 1.0 | Strong | | |

Abbreviation: RBM, Radial Breathing Mode.

argon concentrations. In order to determine the carbon nanotube diameter, the Raman shift intensities were utilized and, based on the values in the table, we determined the diameter to be 1.0 nm, so that $\Delta 1$ was calculated as $\Delta 1$ ~0.45/d (nm) eV.²¹ Contact resistance was measured in saturation current, and we obtained approximately 100 k Ω in this device.

Simulation was performed at room temperature, using MATLAB (MathWorks, Natick, MA, USA), on the device for different values of V_{SD} and different V_G variances. For the device, $t_{\alpha x}$ =300 nm and we used fitting parameters α_0 =0.992, α_1 =-0.05 V⁻¹ and α_s =0.024 V⁻².

Figure 5A–C display curve modeling for V_G between –2.5 and +2.5 V, –5.0 and +5.0 V, and –10.0 and +10.0 V, respectively, and for V_{SD} equal to 0.03 V, 0.02 V, and 0.01 V. The results highlight how the gate-source voltage sweep affects hysteresis parameters V_C and w. A larger sweep enlarges w and shifts V_C toward negative values of V_G , while changing V_{SD} does not affect these parameters. It is noted that the bottom curves of the model do not reach the same value of the upper curves on negative voltage limit, and the reason we suggest is that the devices did not reach their maximum saturation current, and, for this, the negative voltage limit should be lower. Despite this observation and some inaccuracies due to measurement and parameter deviation, a good fitting could be observed in all graphs.

This work makes some contributions regarding CNT-FET modeling: first, simulations with higher biases of V_G were performed, while several articles modeling CNTFET devices used a smaller gate voltage sweep (eg, 0 to +0.05 volts) in simulations, in comparison to our work, and second, the description of hysteresis effect by using L²P parameters showed that hysteretic loop width and shift is sensitive to gate voltage bias.

In order to evaluate the accuracy of the proposed model, three other devices were submitted to measures, for V_G between $-10~\rm V$ and $+10~\rm V$, with the same procedures and conditions

Liu et al Dovepress

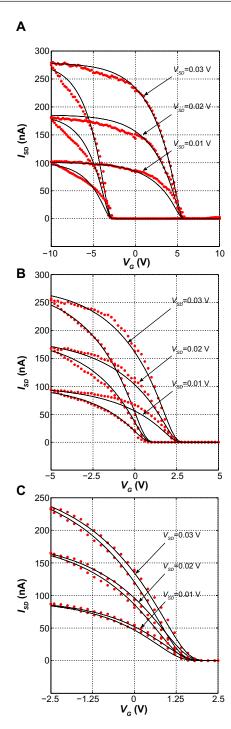


Figure 5 Comparison between experimental (red dot) and model (line) curves, for V_{co} =0.03 V, 0.02 V, and 0.01 V.

Notes: V_c ranged from (**A**) -10 V to +10 V; (**B**) -5 V to +5 V; and (**C**) -2.5 V to +2.5 V. The variables used are the drain current (I_{SD}), the gate voltage (V_c) and the source/drain voltage (V_{SD}).

described earlier in the "Experimental procedure" section. Subsequently, the experimental results were employed in simulations for the modeling of the devices. Table 2 describes the parameters used for the devices and the relative error of the comparison between the experimental and model curves. It is noted that, with the results shown in Table 2, the model

Table 2 Comparison of parameters and relative error among tested devices

| Device number | V _{SD} (V) | $\alpha_{_{0}}$ | α _ι (V ⁻¹) | α ₂ (V ⁻²) | w | V _c | Relative error (%) |
|------------------|---------------------|-----------------|-----------------------------------|-----------------------------------|-----|-----------------------|-----------------------|
| I | 0.01 | 0.988 | -0.03 | 2.00 | 6.8 | 3.4 | 4.8 |
| | 0.02 | | | | | | 3.4 |
| | 0.03 | | | | | | 4.8 |
| 2 | 0.01 | 0.990 | -0.0 I | 1.10 | 7.0 | 2.0 | 4.8 |
| | 0.02 | | | | | | 5.5 |
| | 0.03 | | | | | | 5.8 |
| 3 | 0.01 | 0.990 | -0.04 | 0.15 | 6.4 | 3.4 | 5.7 |
| | 0.02 | | | | | | 4.8 |
| | 0.03 | | | | | | 2.4 |

Notes: $V_{_{5D}}$ is the voltage between the drain and the source of the CNTFET; $\alpha_{_0}$, $\alpha_{_1}$ and $\alpha_{_2}$ are the fitting parameters specified in the model description; w and $V_{_C}$ are parameters referent to the hysteresis effect in the device, explained in the model description as well. The relative error is between the modeled curve and the curve that represents the real data acquired, for each case.

is applicable to other devices with different characteristics and behavior. In spite of the expected relative errors, since the measurement accuracy and model approximations might interfere in the modeling, these differences do not attenuate the effectiveness of the proposed work.

Conclusion

In this work, we successfully modeled $I_{\rm SD}{-}V_{\rm G}$ curves including hysteresis effects, for different voltage values and parameters, as a result of mathematical adaptations over the main expression, respecting the physical concepts of ballistic theory. The L²P model contributed to the characterization, as we could use its parameters to distinguish the two curves caused by hysteresis. The modeling brings detailed information about the device behavior, based on its characteristics.

Currently, we are studying improvements in the characterization process. One improvement that we intend to demonstrate in a future work is the prior identification of the hysteretic parameters without using graphic methods. Nonetheless, the significant contribution presented in this article is that, given a device with its parameters, it is possible to mathematically localize a bias point over the experimental curves within a desired region of operation, thereby permitting accurate control of the CNTFET for specific applications, such as nonvolatile memory devices.

Acknowledgments

This work was supported by the CNPq (Process 471864/2011-0). The authors (Mateus S Moura and Marcio Fontana) acknowledge the Department of Education (Ministério da Educação, MEC), through the Secretariat of Higher

Education (Secretaria de Educação Superior, SESu), for the support of the Tutorial Education Program (Programa de Educação Tutorial, PET) of the Electrical Engineering degree from the Federal University of Bahia (Universidade Federal da Bahia). The authors also thank P Barbara for insightful discussions on hysteresis.

Disclosure

The authors report no conflicts of interest in this work.

References

- Pushkarna A, Raghavan S, Mahmoodi H, ed. Comparison of performance parameters of SRAM designs in 16 nm CMOS and CNTFET technologies. SOC Conference (SOCC), 2010 IEEE International; September 27–29, 2010; Las Vegas, NV: SOCC; 2010.
- Guo J, Datta S, Lundstrom M, et al, ed. Assessment of silicon MOS and carbon nanotube FET performance limits using a general theory of ballistic transistors. International Electron Devices Meeting, 2002.
 IEDM '02. International; December 8–11, 2002; San Francisco, CA: The Institute of Electrical and Electronics Engineers; 2002.
- Tans SJ, Verschueren ARM, Dekker C. Room-temperature transistor based on a single carbon nanotube. *Nature*. 1998;393:49–52.
- Robert-Peillard A, Rotkin SV. Modeling hysteresis phenomena in nanotube field-effect transistors. *IEEE Trans Nanotechnol.* 2005;4(2):284–288.
- de Almeida LAL, Deep GS, Lima AMN, Neff H. Limiting loop proximity hysteresis model. *IEEE Trans Magn*. 2003;39(1):523–528.
- Mayergoyz ID. Mathematical Models of Hysteresis. New York, NY: Springer-Verlag; 1991.
- Jiles DC, Atherton DL. Ferromagnetic hysteresis. *IEEE Trans Magn*. 1983;19(5):2183–2185.
- Raychowdhury A, Mukhopadhyay S, Roy K. A circuit-compatible model of ballistic carbon nanotube field-effect transistors. *IEEE Transactions* on Computer-Aided Design of Integrated Circuits and Systems. 2004;23(10):1411–1420.

- Lundstrom M, Ren Z, Datta S. Essential physics of carrier transport in nanoscale MOSFETs. *IEEE Trans Electron Devices*. 2002;49(1): 133–141.
- Javey A, Guo J, Wang Q, Lundstrom M, Dai H. Ballistic carbon nanotube field-effect transistors. *Nature*. 2003;424:654

 –657.
- Dai H, Javey A, Pop E, Mann D, Kim W, Lu Y. Electrical transport properties and field-effect transistors of carbon nanotubes. *Nano: Brief Reports and Reviews*. 2006;1(1):1–13.
- 12. Yang Y, Fedorov G, Barbara P, et al. Coherent nonlocal transport in quantum wires with strongly coupled electrodes. *Physical Review B Condensed Matter and Materials Physics*. 2013;87(4).
- Pregaldiny F, Lallement C, Kammerer J. Design-oriented compact modes for CNTFETs. DTIS 2006. International Conference on Design and Test of Integrated Systems in Nanoscale Technology; September 5–7, 2006; Tunis, Tunisia: The Institute of Electrical and Electronics Engineers, 2007.
- Aouaj A, Bouziane A, Nouacry A. Nanotube carbon transistor (CNT-FET), I-V and C-V, a qualitative comparison between fettoy simulator and compact model. ICMCS '09. International Conference on Multimedia Computing and Systems; April 2–4, 2009; Ouarzazate, Morocco: 236–239.
- Fuhrer MS, Kim BM, Durkop T, Brintlinger T. High-mobility nanotube transistor memory. Nano Lett. 2002;2(7):755–759.
- Di Bartolomeo A, Rinzan M, Boyd AK, et al. Electrical properties and memory effects of field-effect transistors from networks of singleand double-walled carbon nanotubes. *Nanotechnology*. 2010;21(11): 115204
- Di Bartolomeo A, Yang Y, Rinzan M, Boyd AK, Barbara P. Record endurance for single-walled carbon nanotube-based memory cell. *Nanoscale Res Lett.* 2010;5(11):1852–1855.
- 18. Tersoff J. Contact resistance of carbon nanotubes. *Appl Phys Lett.* 1999;74(15): 2122–2124.
- Zhou J, Barbara P, Paranjape M. Novel in-situ decoration of singlewalled carbon nanotube transistors with metal nanoparticles. *J Nanosci Nanotechnol*. 2010;10(6):3890–3894.
- Dresselhaus MS, Dresselhaus G, Saito R, Jorio A. Raman spectroscopy of carbon nanotubes. *Phys Rep.* 2005;409(2):47–99.
- McEuen PL, Fuhrer MS, Park H. Single-walled carbon nanotube electronics. *IEEE Trans Nanotechnol*. 2002;1(1):78–85.

Nanotechnology, Science and Applications

Publish your work in this journal

Nanotechnology, Science and Applications is an international, peerreviewed, open access journal that focuses on the science of nanotechnology in a wide range of industrial and academic applications. It is characterized by the rapid reporting across all sectors, including engineering, optics, bio-medicine, cosmetics, textiles, resource sustainability and science. Applied research into nano-materials, particles, nanostructures and fabrication, diagnostics and analytics, drug delivery and toxicology constitute the primary direction of the journal. The manuscript management system is completely online and includes a very quick and fair peer-review system, which is all easy to use.

 $\textbf{Submit your manuscript here:} \ \texttt{http://www.dovepress.com/nanotechnology-science-and-applications-journal} \\$

