ORIGINAL RESEARCH

Power optimized variation aware dual-threshold SRAM cell design technique

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Abstract: Bulk complementary metal-oxide semiconductor (CMOS) technology is facing enormous challenges at channel lengths below 45 nm, such as gate tunneling, device mismatch, random dopant fluctuations, and mobility degradation. Although multiple gate transistors and strained silicon devices overcome some of the bulk CMOS problems, it is sensible to look for revolutionary new materials and devices to replace silicon. It is obvious that future technology materials should exhibit higher mobility, better channel electrostatics, scalability, and robustness against process variations. Carbon nanotube-based technology is very promising because it has most of these desired features. There is a need to explore the potential of this emerging technology by designing circuits based on this technology and comparing their performance with that of existing bulk CMOS technology. In this paper, we propose a low-power variation-immune dual-threshold voltage carbon nanotube field effect transistor (CNFET)-based seven-transistor (7T) static random access memory (SRAM) cell. The proposed CNFET-based 7T SRAM cell offers ~1.2× improvement in standby power, ~1.3× improvement in read delay, and ~1.1× improvement in write delay. It offers narrower spread in write access time (1.4× at optimum energy point [OEP] and 1.2× at 1 V). It features 56.3% improvement in static noise margin and 40% improvement in read static noise margin. All the simulation measurements are taken at proposed OEP decided by the optimum results obtained after extensive simulation on HSPICE (high-performance simulation program with integrated circuit emphasis) environment.

Keywords: carbon nanotube field effect transistor (CNFET), chirality vector, random dopant fluctuation (RDF), SNM

Introduction

The continuous growth of recent mobile and portable devices and applications has caused a tremendous thrust for low power circuit design. Static random access memory (SRAM) is a highly used circuit in modern processors and occupies a considerable portion of chip area. It is a major contributor to the total power consumption. Various methods and techniques, such as SRAM's cell voltage collapsing, increasing virtual ground,[1–3] have been applied successfully in the low power and performance region of the design spectrum. However, in some applications where ultralow power consumption is the primary requirement and performance is of secondary importance, a more aggressive approach is warranted. Such applications range from various medical applications (such as implantable pacemakers, defibrillators, hearing aids) to the emerging mobile applications (such as wearable wristwatch computers, wireless sensor nodes, radio-frequency identification [RFID] tags). However, such minimum

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energy operation is only possible in the subthreshold region. The pitfall of subthreshold design and near-threshold computing is increased sensitivity to parameter variation. These fluctuations are more pronounced in minimum-geometry devices commonly used in area-constraint circuits such as SRAM cells.[4] The static noise margin (SNM) model[5] assumes identical device threshold voltage across all cell transistors, making it unsuitable for predicting the effects of threshold voltage mismatch between adjacent transistors within a cell due to random dopant fluctuation (RDF). Therefore, reinvestigation is required to reassess SNM in scaled technologies to ensure stability of the SRAM cell. Process, voltage, and temperature (PVT) variations can be mitigated by the adaptive body biasing design technique,[6] but its effect diminishes with technology scaling.[7] SRAM is a highly used circuit of modern chips. As per the prediction of the International Technology Roadmap For Semiconductors (ITRS), an embedded cache will occupy 90% of a system on a chip by 2013.[8] Hence, the design and reinvestigation of the SRAM cell in terms of its design metrics is not only vital, but its robustness against PVT variations is necessary in a nanoscale regime such as 22 nm technology node.

Research over the past 5 years has demonstrated that the minimum-energy point (MEP) of the energy-delay curve is attractive. The penalty for operating at the MEP is substantial. We can gain 10× in performance by increasing energy by 20% above MEP. The most dominant optimization variable around MEP is the supply voltage.[9] We explored the design space above MEP and below V_{DD} (supply voltage) to achieve higher performance at the cost of minimal delay. In this paper, we make the following contributions:

1. In view of the aforesaid ultralow power requirement and variation issue, we propose a fully differential dual-diameter carbon nanotube field effect transistor (CNFET)-based seven-transistor (7T) SRAM cell (hereafter called CNFET-7T) and compare its performance at proposed optimum energy point (OEP), defined as low-power dissipation point, with its complementary metal-oxide semiconductor (CMOS) counterpart.

2. We demonstrate that the proposed design outperforms its CMOS counterpart CMOS-based 7T SRAM cell (hereafter called 7T) in terms of static noise margin (SNM) and read-static-noise margin (RSNM).

3. We establish that the proposed design offers improved write access time variation exhibiting its immunity against PVT variation. This is achieved by proper selection of chirality vector for appropriate transistor in the proposed design.

4. In standby mode, SRAM cells are inactive and consume power for data retention due to various leakage components. We investigate leakage power consumed by proposed design and 7T.

Estimation of threshold voltage of CNFET

Sixty-five nanometer technology became common after 2006, and 45 nm technology was announced in 2007. As CMOS continues to scale deeper into the nanoscale, various nonidealities cause the I–V characteristics of nanoscaled devices to be substantially different from that of long-channel devices. It becomes more difficult to further improve device/circuit performance by reducing the physical gate length. As CMOS reaches its scaling limits, development of alternative technologies is necessary to further improve device/circuit performance by reducing the physical gate length.[10] Nanotechnology-based fabrication is expected to offer the extra density and potential performance to take electronic circuits to the next step. Several nanoscale electronic devices have been demonstrated in the recent past by researchers, some of the most promising being CNFET. The CNFETs can be scaled down to 10-nm channel length and 4-nm channel width, thereby enhancing throughput in terms of speed and power compared with metal-oxide-semiconductor field-effect transistor (MOSFET). The shortcoming of the CNFET-based design is that there are some fabrication issues, which are likely to be overcome in the near future. The performance of CNFET has significantly improved since the first fabricated device in 1998. Most of the fabrication issues like positioning and alignment of carbon nanotubes (CNTs) along with the presence of metallic CNTs have been solved.[11–15] The impact of CNT diameter and source/drain doping variations is not significant.[16,17] Moreover, CNFET can be fabricated using the existing silicon MOSFET infrastructure and it can also be integrated with silicon MOSFET on the same chip.[18] Most of the fabrication issues have been solved and CNFET technology is promising. It is also important to investigate the potential of systems designed in upcoming technology for their rapid commercialization once the technology matures.

Most of the fundamental limitations of traditional silicon MOSFETs are mitigated in CNFET. With ultralong (~1 μm) mean free path for elastic scattering, a ballistic or near-ballistic transport can be obtained with the use of CNTs under low voltage bias to achieve the ultimate device performance.[19–21] Its quasi-1D structure provides better electrostatic control over the channel region than 3D devices

(for example, bulk CMOS) and 2D device (for example, fully depleted SOI (silicon on insulator)) structures.[22] Ballistic transport operation and low I_{OFF} (OFF-current) make the CNFET a suitable device for high performance and increased integration. CNTs are categorized into single-walled CNTs (SWCNTs) and multiwalled CNTs (MWCNTs). Most SWCNTs have a diameter of close to 1 nm, with a tube length that can be many millions of times longer. The structure of a SWCNT can be conceptualized by wrapping a 1-atom-thick layer of graphite called graphene into a flawless cylinder. SWCNT-based CNFETs are used in this design.

Properties of a SWCNT depend on its chirality (n_1, n_2): the direction in which it is rolled up. The CNT acts as metal if $n_1 = n_2$ or $(n_1 - n_2)/3 = i$, where i is an integer. Otherwise, the CNT works as semiconductor. The D_{CNT} (diameter of CNT) is estimated using its chirality vector (n_1, n_2) as:[23–26]

$$D_{CNT} = \frac{a}{\pi} \sqrt{n_1^2 + n_2^2 + n_1 n_2} \qquad (1)$$

The V_t (threshold voltage) of CNFET can be approximated to the first order as the half bandgap, which is an inverse function of the CNT diameter (D_{CNT}):[23]

$$V_t \approx \frac{E_g}{2q} = \frac{1}{\sqrt{3}} \frac{aV_\pi}{qD_{CNT}} \qquad (2)$$

where E_g = energy gap, q = electronic charge, $a = \sqrt{3}d$ = 2.49 Å is the lattice constant (where $d \approx 1.44$ Å is the inter-carbon-atom distance) and $V_\pi = 3.033$ eV is the carbon π–to-π bond energy in the tight bonding model. The use of appropriate D_{CNT} and hence V_t of CNFETs is a critical piece of our design strategy. In this work, dual-V_t and dual-diameter CNFETs are used using chiral vector values (11, 0) and (13, 0). The D_{CNT} of the CNFET with chiral vector value (11, 0) and (13, 0) are computed using (1) to be 0.8719 nm (MP1, MP2, MN1, MN2 and MN4 of CNFET-7T) and 1.03 nm (for MN3 and MN5 of CNFET-7T) respectively. The V_t of the CNFET with chiral vector value of (11, 0) and (13, 0) are computed using (2) to be 0.5018 V and 0.4246 V respectively.

Compared with CMOS circuits, the CNFET circuits with 1–10 CNTs per device is about 2 to 10 times faster.[10,25] CNTs are placed on substrate having a dielectric constant of $K_{sub} = 4$. The tubes are separated by a high-k (Hi-k) material called HfO_2 (hafnium oxide) having a dielectric constant of $K_{ox} = 16$ and thickness of $t_{ox} = 4$ nm. Other important device and technology parameters related to CNFET are tabulated in Table 1. The I–V characteristics of employed CNFETs with chirality vector (11, 0) and (13, 0) and NMOS (n-type metal-oxide-semiconductor) with zero bias threshold

Table 1 Device and technology parameters of CNFET

Parameter	Description	Value
L_{ch}	Physical channel length	22 nm
W_g	The width of metal gate (sub_pitch)	6.4 nm
K_{ox}	Dielectric constant of high-K gate oxide	16
(n_1, n_2)	Chirality of the tube	(11, 0) (13, 0)
n_CNT	Number of tube	1

voltage, $V_{tn0} = 0.63$ V are plotted in Figure 1. P-type CNFET used in the proposed design has I–V characteristics with opposite polarity (not shown). The threshold voltages of N-CNFET are estimated using (1) and (2) with chirality vector ranging from (7, 0) to (36, 0). First, the D_{CNT} are estimated substituting the value of the constant π = 3.142, the value of the lattice constant $a = 2.49$ Å, and the value of n_1 ranging from 7 to 36 keeping $n_2 = 0$. Next, the threshold voltage V_t is estimated substituting the value of $a = 2.49$ Å, the value of the carbon π–π bond energy $V_\pi = 3.033$ eV, the value of electronic charge $q = 1.6 \times 10^{-19}$ C, and the estimated value of D_{CNT}. The estimated values of threshold voltage for each value of n_1 ranging from 7 to 36 are plotted in Figure 2. The plot in Figure 2 shows two end points with $V_t = 0.78857$ V at $n_1 = 7$ and $V_t = 0.153$ V at $n_1 = 36$. Two other important points in this plot are (11, 0.5018) and (13, 0.4246) which indicate $V_t = 0.5018$ V at $n_1 = 11$ and $V_t = 0.4246$ V at $n_1 = 13$. These are the threshold voltages of CNFETs used in the proposed design. The threshold voltage (V_t) of P-type CNFET employed in this design has an opposite polarity.[27]
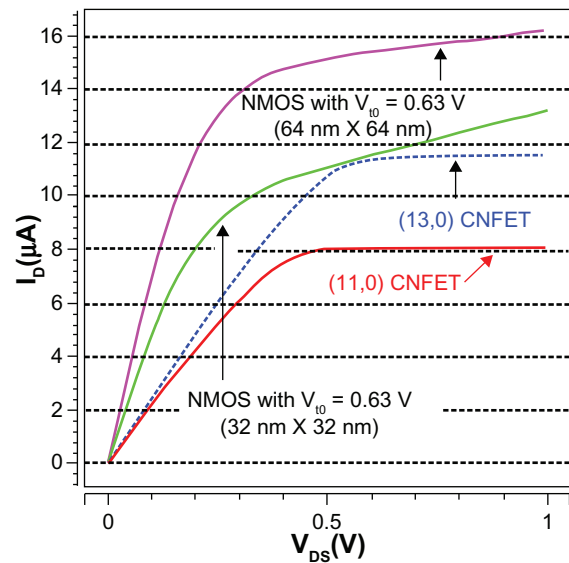

Figure 1 Comparison of I–V characteristics of NMOS and CNFET.
Abbreviations: CNFET, carbon nanotube field effect transistor; NMOS, n-type metal-oxide-semiconductor.
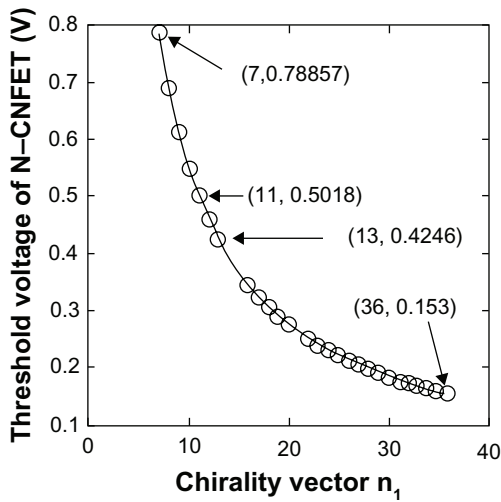
Figure 2 Threshold voltage (V_t) versus chirality vector (n_1).
Abbreviation: CNFET, carbon nanotube field effect transistor.

Proposed CNFET-based 7T SRAM cell

Aly et al[28] proposed a CMOS-7T SRAM cell similar to the proposed CNFET-7T shown in Figure 3 (or Figure 4), basically to reduce the activity factor α_{BL} for reduction of dynamic power while writing to a cell given by $P_{WRITE} = \alpha_{BL} \times C_{BL} \times V^2_{DD} \times F_{WRITE}$, where α_{BL} is the switching activity factor for writing, C_{BL} is the bitline capacitance, V_{DD} is the supply voltage, and F_{WRITE} is the writing frequency to the SRAM cell. But static power consumption in a SRAM cell is more critical than dynamic power consumption, since whole parts of the cache remains idle most of the time except the row being accessed. Therefore, this paper proposes implementation of 7T SRAM with CNFET operating at OEP and demonstrates that the proposed design is better in terms of standby power dissipation.
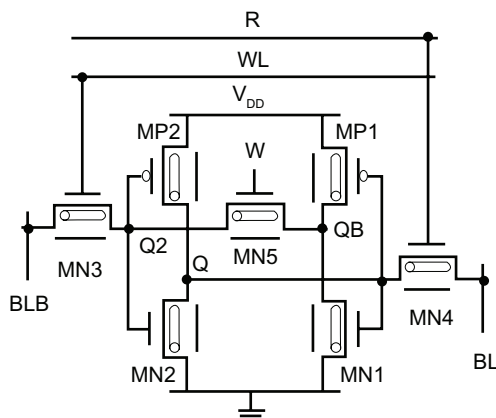

Figure 3 CNFET-based 7T SRAM cell.
Abbreviation: CNFET, carbon nanotube field effect transistor; SRAM, static random access memory.
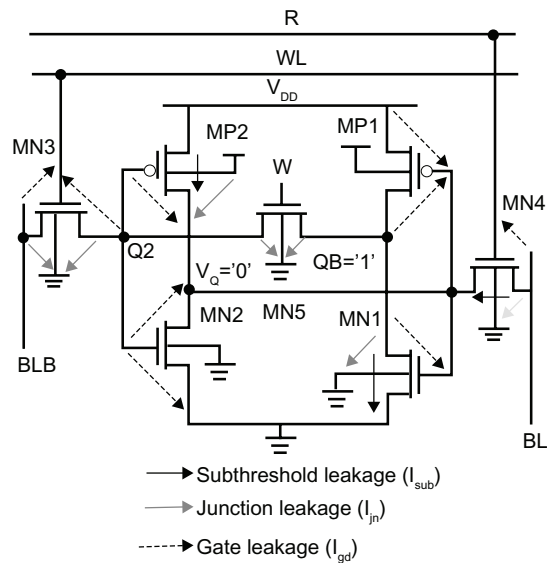

Figure 4 Leakage components in 7T SRAM cell.
Abbreviations: 7T, seven-transistor; SRAM, static random access memory.

Read/write operation

Both BL and BLB are precharged high before and after each read/write operation. The write operation in the 7T/CNFET-7T cell starts by turning MN5 off. Complement of data to be written to node Q is applied to BLB and MN3 is turned on by asserting WL high, leaving MN4 off. BL and MN4 do not take part in the write operation. During standby mode, MN3 and MN4 are kept off applying WL and R low, MN5 is kept on asserting W high. During read operation with QB storing "0", BLB discharges through the critical read path consists of MN3, MN5, and MN1. BL discharges through the read path MN4 and MN2 during read operation with Q storing "0". Main device and technology parameters for 7T cell used for comparison with the proposed design are tabulated in Table 2. As MN1 ≥ 3 and MN2 ≥ 2 ensure stable read operation,[28] the transistors in the 7T cell are sized as shown in Table 2. The 7T also requires low-V_t MN5. To avoid extra masking cost and to fulfill this requirement, the diameter of MN5 is increased to reduce its V_t in the proposed design. Other devices used for the design are square transistors with

Table 2 Device and technology parameters of CMOS-based 7T

Parameter	CMOS-based 7T
V_{tn0}	0.63 V
V_{tp0}	−0.5808 V
MP1, MP2	W = 22 nm, L = 22 nm
MN1	W = 66 nm, L = 22 nm
MN2	W = 44 nm, L = 22 nm
MN3, MN4, MN5	W = 22 nm, L = 22 nm

Abbreviations: CMOS, complementary metal-oxide semiconductor; 7T, seven-transistor; W, width; L, length.

minimum channel length. This work implements CMOS-based 7T SRAM cell using dual-diameter dual-V_t CNFETs, and its performance is assessed at OEP.

To investigate the performance in terms of various design metrics, extensive simulations are run on HSPICE (high-performance simulation program with integrated circuit emphasis), and finally CNFETs with two different diameters are selected to achieve optimum results. HSPICE has been an industry-standard circuit simulator for the past 30 years with an error of less than 5%. As mentioned earlier, the diameter selected for MN3 and MN5 is 1.03 nm to increase its drive current, as drive current through CNT is proportional to its diameter. This has resulted in reduction of read and write delays, which are shown later. The diameter of the other five transistors is selected to be 0.8719 nm. The values of device diameters, threshold voltages, and the corresponding chirality vectors are tabulated in Table 3. As mentioned earlier, single-tube CNFETs are used in this work.

Simulation results and comparisons

We present measurements of various design metrics which are measured during simulation on HSPICE using experimentally validated CNFET model,[23] and 22 nm CMOS Berkeley Predictive Technology Model (BPTM).[29] The CNFET model has been calibrated to 90% accuracy with experimental data (AC and DC characteristics) from fabricated CNFET circuits.[30]

Standby power

The leakage current is the major contributor to the total power consumption in SRAM cell in nanoscaled technology. The total leakage current in a SRAM cell is mainly (neglecting minor components such as I_{GIDL} and $I_{punchthrough}$) due to subthreshold-leakage current (I_{sub}), the gate-leakage current (I_{gate}) and the reverse-biased drain- and source-body junction band-to-band tunneling (BTBT) leakage current (I_{jn}) through different transistors as shown in Figure 4:[31–33]

$$I_{sub} = I_{sub\,MN4} + I_{sub\,MN1} + I_{sub\,MP2}$$

$$I_{jn} = 2I_{jn\,MN3} + I_{jn\,MN4} + I_{jn\,MN1} + I_{jn\,MP2} + 2I_{JN\,MN5}$$

$$I_{gate} = I_{gd\,MN3} + I_{gs\,MN3} + I_{gd\,MN4} + I_{gd\,MP2} \\ + I_{gd\,MN2} + I_{gs\,MN2} + I_{gd\,MP1} + I_{gs\,MP1} + I_{gd\,MN1}$$

$$I_{leak} = I_{sub} + I_{jn} + I_{gate} \qquad (3)$$

Figure 4 shows the various leakage components in 7T, with storage node Q and QB storing the values as indicated. The S_{PWR} (standby power) consumed due to these leakage

Table 3 Device parameters of proposed design

CNFETs	Chirality vector	Threshold voltage (V)	Diameter (nm)
MP1, MP2, MN1, MN2, MN4	(11, 0)	|0.5018|	0.8719
MN3, MN5	(13, 0)	0.4246	1.03

Abbreviation: CNFET, carbon nanotube field effect transistor.

currents is measured at various voltage points starting from $V_{DD} = 1$ V to the minimal voltage of $V_{DD} = 857$ mV and 660 mV for 7T and CNFET-7T respectively. As the cell is asymmetrical, the measurement is done under two conditions with storage node Q storing "0" and Q storing "1" because it is evident from Figure 4, that the leakage components, and thus the current equation differ depending on stored value at Q and QB.

The measured results are averaged and the mean values are plotted in Figure 5, where important measurement points are marked with arrows. Compared with 7T (operating at $V_{DD} = 1$ V consuming 61.94 pW), the CNFET-7T (operating at 1V consuming 57.73 pW) saves 1.073× standby power. As observed from Figure 5, the 7T consumes 38.54 pW whereas CNFET-7T consumes 33.63 pW at iso-operating voltage of 857 mV. Therefore even if the proposed design is operated at the minimum operating voltage of 7T (ie, $V_{DD} = 857$ mV) there is a saving in S_{PWR} by 1.146×. This is attributed to the higher leakage current components in MOSFET compared with CNFET. That is, OFF-current of CNFET is much lower than that of MOSFET. As illustrated in Figure 5, if the CNFET-7T is operated at 660 mV, there will be a substantial amount of saving in S_{PWR}.

Under the measuring condition used (with equal wordline slew rate and on time), 7T could be operated up to 857 mV and CNFET-7T could be operated up to 660 mV without
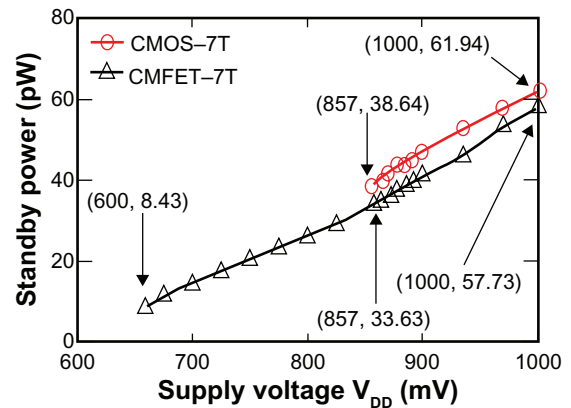
Figure 5 Standby power (S_{PWR}) measured with Q storing "0".
Abbreviations: CMOS, complementary metal-oxide semiconductor; CNFET, carbon nanotube field effect transistor.

facing read and write failure. If the measuring condition is changed, both the design can be operated even in the near subthreshold region. Particularly, CNFET-7T can be operated in subthreshold region without failure. However, the designs are operated in the superthreshold region to explore OEP in this region without compromising much with delay penalty. The iso-operating voltage, ie, 857 mV, is found to be OEP, without incurring much delay in accessing the cell. V_{DD} can be further scaled down for CNFET-7T for improved results.

Read/write access time

Figure 6 shows the read access time (T_{RA}) versus V_{DD} plot. The T_{RA} is estimated as the time required for developing a voltage differential to be sensed by the sense amplifier (not shown) from the point when WL reaches 50% of its full swing from its initial low level to the point when BL/BLB falls by 10% of its full swing from its initial high value. As the cell is asymmetrical, the measurement is done under two conditions – with storage node Q storing "0" and Q storing "1" and the results are averaged before plotting. It is observed from Figure 6 that the read delay of 7T at iso-operating voltage of 857 mV is 1.321× compared with CNFET-7T.

Figure 7 shows the write access time (T_{WA}) versus V_{DD} plot. While writing "0" to Q, BLB is raised high and the write operation is completed after two inverter delays when QB settles to its new state. Therefore, this operation takes quite a long time compared with the read operation. MN3 of CNFET-7T is of low-V_t. Therefore, it passes a higher voltage to the gate of MN2 driving it harder (compared with 7T) both in cases of reading as well as writing, thereby reducing the read/write delay. The CNFET-7T offers 1.066× improvement in write delay at iso-operating voltage of V_{DD} = 857 mV. As observed from Figures 5 and 6, operation of CNFET-7T
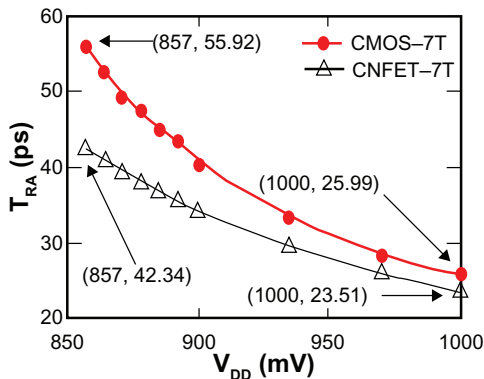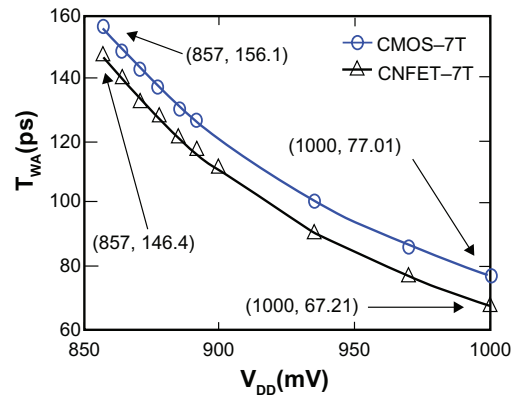

Figure 7 Write access time versus V_{DD}.
Abbreviations: CMOS, complementary metal-oxide semiconductor; CNFET, carbon nanotube field effect transistor.

at OEP instead of V_{DD} = 1 V offers 41.7% improvement in S_{PWR} incurring 44.5% penalty in T_{RA}, whereas operation of 7T at OEP instead of V_{DD} = 1V offers 37.8% improvement in S_{PWR} incurring 53.5% penalty in T_{RA}. Therefore, the proposed design is superior to its CMOS counterpart in terms of most of its major design metrics discussed so far.

Write access time variation

We present variation measurements of write-access time (T_{WA}), which is measured during simulation on HSPICE. Monte Carlo simulations are performed for the measurements. Monte Carlo simulation is a method for iteratively evaluating a design. The goal is to determine how random variation on process parameters, voltage, and temperature affects the performance and reliability of a design. The standard deviation (σ) is a measure of dispersion (or variability) that states numerically the extent to which individual observations vary on average. Figure 8 plots the normalized standard deviation of T_{WA} of the two designs at OEP (V_{DD} = 0.857 V) and V_{DD} = 1V. It is observed from the figure that the proposed design shows 1.4× less variation in write access time at 0.857 V and 1.2× at 1 V. This shows the robustness of the

Figure 6 Read access time versus V_{DD}.
Abbreviations: CMOS, complementary metal-oxide semiconductor; CNFET, carbon nanotube field effect transistor.
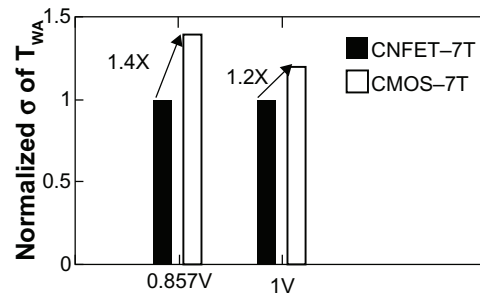

Figure 8 Write delay variation measurement.
Abbreviations: CMOS, complementary metal-oxide semiconductor; CNFET, carbon nanotube field effect transistor.

proposed design against PVT variations. Ideally I_D is supposed to be constant in saturation region. However, in practice, increasing V_{DS} (drain-to-source voltage) beyond $V_{DS\text{-}sat}$ (drain-to-source saturation voltage) does affect the channel somewhat. As the V_{DS} is increased, the depletion layer widens, thereby reducing the effective channel length. Since I_D is inversely proportional to the channel length, I_D increases with V_{DS}. This DIBL (drain-induced barrier lowering) or SCE (short-channel effect) is more pronounced in small geometry MOSFET, and it has negligible impact on CNFET, which is evident from Figure 1. It clearly shows that the I_D in saturation region is almost constant in case of CNFET, whereas it shows almost linear increase in case of MOSFET. This signifies the variation in I_D with V_{DS}. It is needless to say that during read/write operations node voltages change thereby varying V_{DS} and finally causing variation in T_{WA} and T_{RA}.

Static noise margin measurements

The static noise margin (SNM) of SRAM cell is defined as the minimum DC noise voltage necessary to flip the state of the cell. SNM of an SRAM is a widely used design metric that measures the cell stability. Simulation measurement of SNM is carried out for both the designs. Figure 9 shows a test setup for measuring SNM. Figure 10 plots the combined "butterfly curve" of 7T and proposed CNFET-7T at OEP (iso-operating voltage of $V_{DD} = 857$ mV). The butterfly curve is obtained in the following way using the test circuit: 1) W and bit lines (BL, BLB) are biased at V_{DD} and WL and R is biased at ground; 2) Voltage of N1 is swept from 0 V to V_{DD} while measuring voltage of QB; 3) Voltage of N2 is swept from 0 V to V_{DD} while measuring voltage of Q in the same way; and 4) Measured voltages are plotted to get a butterfly curve. The side length of maximum square that can be embedded within the smaller lobe of the butterfly curve represents the SNM of the cell.
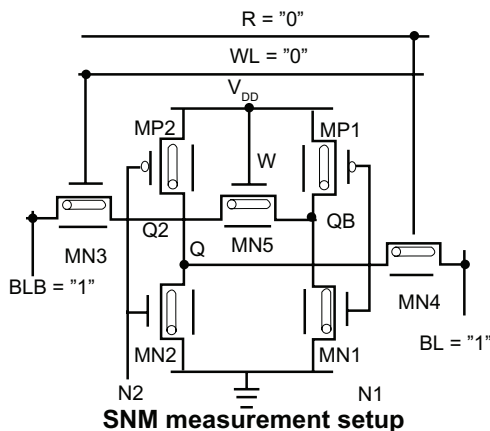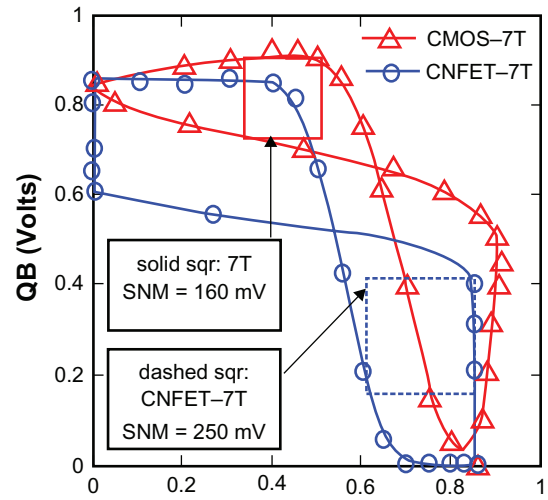

Figure 10 SNM of 7T and CNFET-7T.
Abbreviations: CMOS, complementary metal-oxide semiconductor; CNFET, carbon nanotube field effect transistor; SNM, static noise margin.

This definition holds good because, when the value of noise voltage increases from 0, the VTC (voltage transfer characteristic) for inverter 1 formed with MP1 and MN1 moves to the right and the VTC^{-1} (inverse VTC) for inverter 2 formed with MP2 and MN2 moves downward. Once they both move by the SNM value, the curves meet at only two points and any further noise flips the cell.[34] As observed from Figure 10, the SNM of 7T is 160 mV, whereas that of CNFET-7T is 250 mV, showing 56.3% improvements in CNFET-7T over the 7T cell. To understand why this happens, remember that both the transistors MN1 and MN2 of CNFET-7T have lower V_t, which implies that the switching threshold of both the inverters are lower than that of 7T. This shifts the VTC of inverter 1 to the left and pushes the VTC^{-1} of inverter 2 down making both the lobes of the butterfly curve wider.
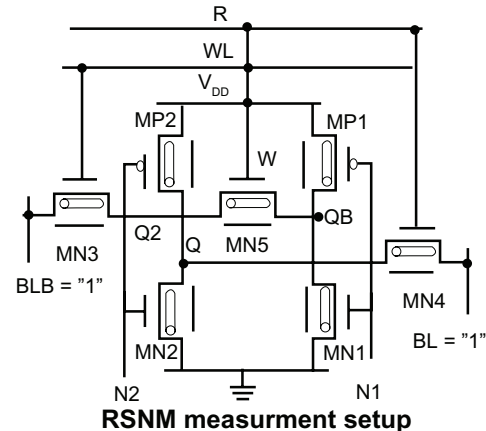

Figure 9 Test setup for measuring static noise margin (SNM).

Figure 11 Test setup for measuring read static noise margin (RSNM).
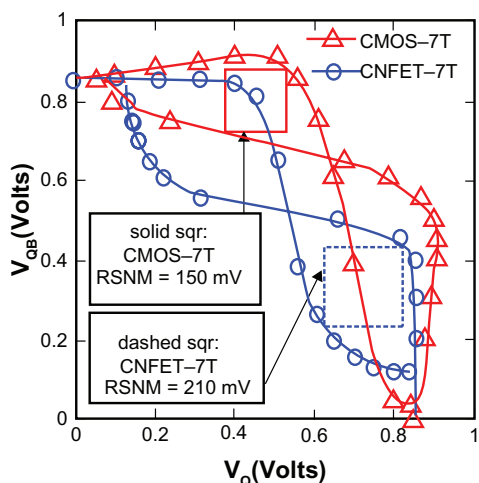
Figure 12 Read static noise margin (RSNM) of 7T and CNFET-7T.
Abbreviations: CMOS, complementary metal-oxide semiconductor; CNFET, carbon nanotube field effect transistor.

Read static noise margin measurements

The SRAM cell is the most susceptible to noise during read operation since the node storing "0" (say, Q in Figure 4) rises to a voltage higher than ground due to a voltage dividing effect between the access transistor (say, MN4) and inverter pull-down NMOS driver (say, MN2). The ratio of the widths of the pull-down transistor to the access transistor, commonly referred to as the cell ratio (CR) or β ratio, decides how high the "0" storage node rises during a read operation. Smaller CRs translate into a larger voltage drop across the pull-down transistor, requiring a smaller noise voltage at the node storing "0" to trip the cell. RSNM is a measure of how much noise voltage is required at the node storing "0" to flip the state of an SRAM cell while reading. Therefore, RSNM is an even more critical design metric of the SRAM cell than SNM. Figure 11 shows a test setup for measuring RSNM. The butterfly curves are obtained with this test setup and using the same measuring technique as done for SNM. Figure 12 plots the combined butterfly curve of 7T and CNFET-7T at OEP. The plot shows that the CNFET-7T outperforms 7T by 40% improvement in RSNM. The reason is obvious from the discussion in the preceding subsection.

Conclusion

We propose a dual-Vt CNFET-based low-power PVT variation immune 7T SRAM cell. We observe during the investigation that the CNFET-based 7T SRAM cell offers better performance in terms of most the design parameters such as standby power and noise margins. The proposed design also shows more robustness against process variations compared with the CMOS-based 7T SRAM cell. This is due to proper

selection of CNFET diameter and hence threshold voltage for appropriate transistors. This is also due to the cylindrical geometry of CNFET. A variation in the gate oxide thickness that strongly affects the drive current and capacitance of CMOS transistors has a negligible impact on the CNFET's operation. We have successfully demonstrated that the proposed design will be effective to reduce standby power, read/write delay, and write delay variation.

Disclosure

The authors report no conflicts of interest in this work.

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